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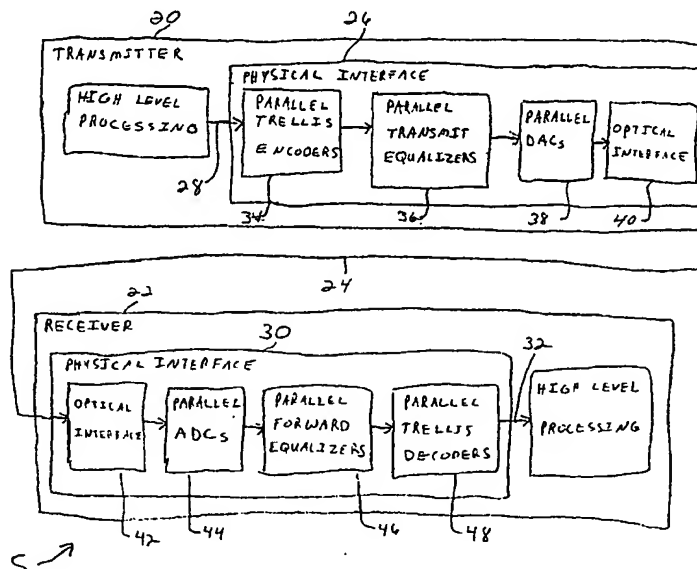
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[Continued on next page]

(54) Title: **SYSTEM AND METHOD FOR HIGH SPEED COMMUNICATIONS USING DIGITAL SIGNAL PROCESSING**



(57) Abstract: Various systems and methods related to equalization precoding in a communications channel are disclosed. In one implementation precoding is performed on signals transmitted over an optical channel. In one implementation precoding and decoding operations are performed in parallel to facilitate high speed processing in relatively low cost circuits. Initialization of the precoders may be realized by transmitting information related to the characteristics of the channel between transceiver pairs.

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1 SYSTEM AND METHOD FOR HIGH SPEED COMMUNICATIONS
 USING DIGITAL SIGNAL PROCESSING

FIELD OF THE INVENTION

5 The invention relates generally to data communications and, more particularly, to systems and methods for performing digital signal processing in a communications system and communication devices.

BACKGROUND OF THE INVENTION

10 The field of data communications relates, in part, to techniques and circuits that facilitate transfer of data over a data channel between components in a communications system. For example, data may be transferred between two computers via a local area network. In addition, data may be transferred within a component. For example, two circuit boards in a communications component such as a switch or a router may communicate via signals routed
15 through a backplane in the switch or the router.

 There is a perpetual need for increased operating speed in data communications systems. On the one hand, developers are continually creating applications that require increasingly greater amounts of data to be sent between system components. On the other hand, end users in general want their applications to run faster which, in turn, often requires that associated data transfers
20 are performed more quickly.

 In an attempt to address the need for faster data communications, various groups have developed standards that specify high speed data transfers between components of data communication systems. For example IEEE standards 802.3ab and 802.3z define Ethernet systems for transferring data at rates up to one gigabit per second (1 Gbit/s). IEEE standard
25 802.3ae defines an Ethernet system for transferring data at rates up to 10 Gbits/s.

 The development of these standards and the ever increasing need for faster data transfers create a need for techniques and circuits capable of achieving high data transfer rates while at the same time providing high reliability over relatively long distances. Moreover, there is an ever present economic motivation to achieve such results in a cost effective manner.
30

SUMMARY OF THE INVENTION

 The invention is directed to data transmission systems and methods incorporating digital signal processing such as equalization precoding and parallel processing to achieve reliable data transmission at relatively high data transfer rates. The invention provides equalization precoding
35 in transmission systems with optical channels and provides parallel processing techniques for optical and non-optical channel systems to increase the speed of the precoding and/or other processing. Moreover, the teachings of the invention may, in substantial part, be implemented in CMOS technology thereby providing a relatively low cost solution.

1 One embodiment of a system constructed according to the invention consists of a transceiver incorporating digital signal processors that process signals to be transmitted and received over a channel. In a transmit section of the transceiver a digital signal processor performs trellis encoding and Tomlinson-Harashima precoding for encoding the signals to be
5 transmitted. In a receive section of the transceiver a digital signal processor performs forward equalization and Viterbi decoding for decoding signals received over the channel.

One embodiment of the transceiver processes signals for an optical channel. Significantly, this embodiment enables relatively high speed data transmission (e.g., 10 Gbits/s) over fiber optic cables such as multimode fiber that have relatively poor performance characteristics. This is
10 accomplished by the precoding scheme which compensates for the characteristics of the optical channel. Thus, this embodiment can provide high speed data transfers over relatively long fiber spans. Significantly, this technique is in many respects more effective than conventional solutions (e.g., restricted mode launch, offset launch and vortex launch) that have been used to overcome bandwidth limitations of fiber optic cables.

15 One embodiment of the transceiver incorporates parallel encoding and decoding for processing signals for optical or non-optical channels. For example, the transmit section performs the trellis encoding and Tomlinson-Harashima precoding in parallel. And the receive section performs the forward equalization and Viterbi decoding in parallel. Significantly, this embodiment can be implemented in relatively low cost CMOS technology, thereby providing
20 high performance with low cost components.

Another embodiment of a system constructed according to the invention incorporates a precoder initialization scheme whereby information related to the characteristics of the channel are transmitted from the receive section of one transceiver to the transmit section of another transceiver at the other end of the channel.

25 BRIEF DESCRIPTION OF THE DRAWINGS

These and other features, aspects and advantages of the present invention will be more fully understood when considered with respect to the following detailed description, appended claims and accompanying drawings, wherein:

30 Figure 1 is a block diagram of one embodiment of a system incorporating equalization precoding for an optical channel in accordance with the invention;

Figure 2 is a block diagram of one embodiment of a transmitter incorporating parallel equalization precoding in accordance with the invention;

35 Figure 3 is a block diagram of one embodiment of a trellis encoder that may be used in the transmitter of Figure 2;

Figure 4 is a block diagram of one embodiment of a Tomlinson-Harashima precoder that may be used in the transmitter of Figure 2;

1 Figure 5 is a block diagram of one embodiment of a receiver that may be used in conjunction with the transmitter of Figure 2;

 Figure 6 is a block diagram of one embodiment of a forward equalizer that may be used in the receiver of Figure 5;

5 Figure 7 is a block diagram of one embodiment of a parallel Tomlinson-Harashima precoder in accordance with the invention;

 Figure 8 is a conceptual block diagram relating to another embodiment of a parallel Tomlinson-Harashima precoder in accordance with the invention;

10 Figure 9 is a block diagram of one embodiment an implementation of the parallel Tomlinson-Harashima precoder of Figure 8;

 Figure 10 is a block diagram of one embodiment of a double row Tomlinson-Harashima precoder in accordance with the invention;

 Figure 11 is a block diagram of another embodiment of a double row Tomlinson-Harashima precoder in accordance with the invention;

15 Figure 12 is a block diagram of another embodiment of a parallel Tomlinson-Harashima precoder in accordance with the invention;

 Figure 13 is a block diagram of one embodiment of a precoder initializer in accordance with the invention;

20 Figure 14 is a block diagram of one embodiment of an analog interface in accordance with the invention;

 Figure 15 is a block diagram of one embodiment of an analog to digital converter in accordance with the invention;

 Figure 16 is a graph of clock jitter specifications for one embodiment of an analog interface in accordance with the invention;

25 Figure 17 is a block diagram of one embodiment of a phase locked loop in accordance with the invention;

 Figure 18 is a block diagram of one embodiment of a voltage controlled oscillator in accordance with the invention;

30 Figure 19 is a schematic diagram of one embodiment of a digital to analog converter circuit and an optical interface circuit in accordance with the invention;

 Figure 20 is a block diagram of one embodiment of a communications system having an electrical physical interface and incorporating transceivers with equalization precoding in accordance with the invention;

35 Figure 21 is a block diagram of another embodiment of a communications system having an electrical physical interface and incorporating transceivers with equalization precoding in accordance with the invention;

 Figure 22 is a block diagram of one embodiment of an optical transceiver module incorporating equalization precoding in accordance with the invention; and

1 Figure 23 is a block diagram of one embodiment of a system incorporating symbol-by-symbol decoding and/or alternative digital signal processing in accordance with the invention.

DETAILED DESCRIPTION OF THE INVENTION

5 The invention is described below, with reference to detailed illustrative embodiments. It will be apparent that the invention can be embodied in a wide variety of forms, some of which may be quite different from those of the disclosed embodiments. Consequently, the specific structural and functional details disclosed herein are merely representative and do not limit the scope of the invention.

10 Figure 1 is a simplified block diagram of one embodiment of a data transmission system S utilizing equalization precoding in accordance with the invention. A transmitter 20 sends data to a receiver 22 over an optical channel 24. In a typical implementation, the transmitter 20 communicates with the receiver 22 according to the International Standard's Organization Open Systems Interconnection (ISO) model. The ISO model defines various protocols for formatting
15 the data. Here, each protocol defines formatting for different stages of transmission ranging from a presentation level (presentation of the data to the end user) to a physical level (transmission of the data over a physical medium). In the OSI context, the invention is primarily concerned with the physical level.

20 In Figure 1, the high level processing in the transmitter 20 formats a data stream to generate packetized data per the OSI model. This data is sent to a transmit physical interface 26, typically via a parallel data bus 28. The transmit physical interface 26 processes the data to a form suitable for transmission over a particular type of channel (e.g., optical). A corresponding receive physical interface 30 in the receiver 22 processes signals received over the channel 24 and presents them via bus 32 to the non-physical layers (e.g., high level processing) for
25 processing per the OSI model.

 In accordance with the invention, the physical interfaces 26 and 30 provide equalization to compensate for the characteristics of the channel 24. Moreover, in this embodiment, the physical interfaces 26 and 30 include parallel structures for performing equalization processing (encoding or decoding) in parallel.

30 The equalization function is at least partially provided in the transmitter portion 20 of the system S. A set of parallel trellis encoders 34 processes data from the data bus 28. A set of parallel transmit equalizers 36 process data from the trellis encoders 34. For example, the output of each trellis encoder may be sent to a unique transmit equalizer. Parallel digital to analog converters (DACs) 38 convert the output of the parallel transmit equalizers 36 to a serial analog
35 stream which drives a transmit optical interface 40.

 On the receiving end of the optical channel 24, a receive optical interface 42 drives parallel analog to digital converters (ADCs) 44. The ADCs 44 provide digital streams to a set of parallel forward equalizers 46. A set of parallel trellis decoders process 48 data from the

1 equalizers 46. For example, the output of each forward equalizer may be sent to a unique trellis decoder.

5 The operation and implementation of the components of Figure 1 will be discussed in more detail in conjunction with the remaining figures. To facilitate a better understanding of these components, the objectives of the embodiment of Figures 2 - 6 will be discussed.

10 This embodiment utilizes five-level pulse amplitude modulation (PAM-5) signaling at 5 gigabaud per second (5 Gbaud/s). The optical channel typically consists of a standard 62.5/125 μ m fiber optic cable with a bandwidth of 160 MHz/500 Mhz · kilometer for 850nm/1310nm lasers, respectively. For example, for a fiber length of 500 meters the bandwidth of the fiber is 1 Ghz for a 1310nm laser.

15 Significantly, the system incorporates adaptive equalization for compensating for intersymbol interference introduced by the limited bandwidth of the multimode fiber. That is, the adaptive equalizer tracks the variations of the laser and fiber response over time and, in response, the system provides appropriate compensation to the signals. For example, the system uses nonlinear equalization to compensate for the nonlinearity of the laser. In this embodiment, the transmit equalizer 36 of Figure 1 is implemented as a Tomlinson-Harashima precoder.

20 Through the use of parallel processing in the transmitter, receiver and data converters, a CMOS integrated circuit constructed according to the invention may achieve a 5 GHz effective sampling rate with a 312.5 MHz actual clock rate. In sum, the embodiment of Figures 2 - 6 uses a 4-dimensional, 8-state, 4-way interleaved Ungerboeck trellis coding and may achieve a coding gain of approximately 6dB over an uncoded PAM-5 system.

25 Referring now to Figures 2 - 6, Figures 2 - 4 depict simplified block diagrams of selected components for a transmitter. Figures 5 - 6 depict simplified block diagrams of selected components for a receiver. These components are described as part of a 10 Gbit/s Ethernet system. In one embodiment, the transmitter and receiver sections described herein are implemented as a transceiver integrated circuit constructed as a single chip.

In the transmitter T of Figure 2, a transmitter section 50 encodes signals received from a media access controller 52 to provide an encoded data stream that drives a laser circuit 54. The laser circuit 54 generates optical signals that are sent over an optical channel (not shown).

30 The basic operation of the media access controller 52 is known in the art and will not be treated in detail here. For a 10 Gbit/s implementation, a data bus 56 from the media access controller 52 to the transmitter section 50 comprises 32 signals, each of which operates at 312.5 MHz.

35 A system interface 58 terminates the signals from the data bus 56 and routes them to a physical coding sublayer 60. In general, the operations of the system interface 58 and the physical coding sublayer 60 are known in the art. For example, the physical coding sublayer 60 performs operations such as scrambling, idle generation, start of stream delimiter insertion and end of stream delimiter insertion.

1 In accordance with one embodiment of the invention, the physical coding sublayer 60 also
incorporates a set of parallel trellis encoders 62. For example, the code may operate in blocks
of sixteen samples with a block rate of $5 \text{ GHz}/16 = 312.5 \text{ MHz}$. This provides an intrinsic
parallelism (by a factor of 16) in both the encoder and the decoder (discussed below), which run
5 at a clock rate of 312.5 MHz. The teachings of the invention may be applied to any number of
levels of parallelism. For example, for a 5 GHz input the system may incorporate eight levels
operating at 625 MHz. In general, the number of parallel levels and the speed at which they
operate will depend on system design goals.

As represented by the designations on the trellis encoders 62, any number of trellis
10 encoders 62 may be used in implementing the teachings of the invention. For the purposes of this
example, the designation "T" is four. Thus, there are four trellis decoders 62 operating in
parallel.

Figure 3 depicts one embodiment of one of the trellis encoders. Each encoder processes
eight of the 32 input signals and outputs four PAM-5 signals. In this embodiment, the encoder
15 62 consists of a 4-dimensional, 8-state Ungerboeck trellis encoder. Thus, the combination of the
four parallel trellis encoders 62 provides 4-dimensional, 8-state, 4-way interleaved Ungerboeck
trellis coding.

The four dimensions consist of four consecutive samples of the signal. For each block of
sixteen samples, the first four samples are processed by the first trellis encoder, the next four
20 samples are processed by the second trellis encoder, and so forth.

Referring again to Figure 2, the outputs of the trellis encoders 64 are routed to a set of
parallel dynamics limited Tomlinson-Harashima precoders 64. As represented by the
designation: "0 ... N-1," any number of precoders may be used in implementing the teachings of
the invention. For the purposes of this example, the designation "N" is sixteen. Thus, in this
25 embodiment there are sixteen precoders operating in parallel.

The operation of one embodiment of one of the Tomlinson-Harashima precoders is
described in conjunction with Figure 4. The precoder is basically, in one embodiment, a filter
with a response equal to the inverse of the response of the channel. For example, if the channel
response has a z-transform $1 + D(z)$, the precoder typically would have a response $1/(1 + D(z))$.
30 Such a precoder 70 and channel 72 are illustrated, for example, in the top half of Figure 4.

In practice, the inverse filter could introduce high gain at some frequencies (where the
channel has high attenuation). This could result in high peak values and high power at the output
of the transmitter. To prevent this, a sequence $v_n = k_n \cdot M$ is added to the transmitted data
sequence x_n . For a PAM-5 alphabet ($x \in \{-2, -1, 0, 1, 2\}$), $M = 5$ and k_n is an arbitrary integer,
35 such that $x_n + v_n$ belong to the extended alphabet $\{\dots, -7, -6, -5, -4, -3, -2, -1, 0, 1, 2, 3, 4, 5, 6, 7, \dots\}$. Here, the specific choice of k_n is made on a symbol by symbol basis with the objective
of minimizing the transmitted power.

1 In traditional Tomlinson-Harashima precoding a wrap-around (or overflow) operation is used to automatically generate v_n . This operation is denoted with the block $\text{mod}(M)$ 74 in the bottom half of Figure 4. When the input is $u_n \geq M/2$, the $\text{mod}(M)$ operation forces y_n to the interval $[-M/2, M/2]$ by adding $k_n \cdot M$ with $k_n < 0$. Similarly, when input $u_n < M/2$, the $\text{mod}(M)$ operation forces y_n to the interval $[-M/2, M/2]$ by adding $k_n \cdot M$ with $k_n > 0$. One will observe that this is the same operation as the two's complement representation of a number u_n when it overflows a register having a word length that allows representing numbers in the interval $[-M/2, M/2]$.

10 The received signal is $x_n + v_n$. A perfectly open eye pattern may be achieved at the input of the receiver (as represented by the hypothetical display device 76). However, the number of levels is larger than in the original alphabet. That is, in a PAM-5 implementation there will be more than five levels at the input of the receiver. To get the desired five levels the slicer determines x_n by finding the value of k_n that makes $x_n + v_n - k_n \cdot M$ fall within the original PAM-5 alphabet $\{-2, -1, 0, 1, 2\}$.

15 In Tomlinson-Harashima precoding k_n can take arbitrary integer values to strictly enforce the condition $-M/2 \leq y_n \leq M/2$. This could result in large values of $x_n + v_n$, the signal at the input of the receiver 78. To reduce the dynamic range of the ADCs, it is desirable to constrain $x_n + v_n$. For example, in a PAM-5 system k may be selected such that $x_n + v_n \in \{-4, -3, -2, -1, 0, 1, 2, 3, 4\}$. This results in a slight increase in the transmit power. However, this also reduces the required resolution of the ADCs.

20 Referring again to Figure 2, the output of each of the sixteen precoders 64 is routed to a set of parallel DACs 68. Again, as represented by the designation: "0 ... N-1," the number of DAC inputs matches the number of precoder outputs. Thus, in this embodiment there are sixteen DAC inputs. The DACs 68 convert the sixteen digital signals to a single 5 Gbaud/s serial stream that drives the laser circuit 54.

25 Referring to Figures 5 - 6, the operation of the receiver will now be discussed. In the receiver R of Figure 5, a photodetector 80 receives optical signals from an optical channel (not shown) to provide an encoded data stream to a receiver section 82. The receiver section decodes the data stream and routes the decoded data to a media access controller 84.

30 In a manner similar to conventional high speed optical receivers, the output of a photodetector 80 is amplified by a preamplifier 86 and filtered by a high pass filter 88. Typically, the high pass filter 88 compensates for baseline wander.

35 The amplitude of the input signal to the set of parallel ADCs 90 is controlled by a programmable gain amplifier 92. The gain of the amplifier 92 is controlled by an automatic gain control 94. Significantly, the combination of the digitally controlled automatic gain control 94 and the analog programmable gain amplifier 92 provides a more effective method of controlling gain for an optical channel. By digitally processing the received optical signals, the gain of the

1 amplifier 92 may be controlled more effectively. This may provide, in part, a method of efficiently utilizing the resolution of the ADCs 90.

5 A timing recovery circuit 96 provides a number of clocks to the components of the receiver R. In this embodiment, f_B , the baud rate clock, runs at 5GHz, f_C is $f_B/16 = 312.5$ MHz and, as discussed below, f_D is a sixteen phase version of f_C . It will be understood that these frequencies are examples and will depend, in part, on the speed of operation of the circuits and the number of parallel circuits in the receiver. For example, in a preferred embodiment eight ADCs will be used, each of which will run at a clock frequency of 625 MHz for a 5 Gbaud/s input signal.

10 The set of parallel ADCs 90 sample the received analog data stream and generate digital signals (e.g., 6 bits per symbol) representative of the analog input signal. In the embodiment depicted, there are sixteen ADCs running at 312.5 Mhz. It will be understood that the number of ADCs and the speed at which they operate will depend on system design goals.

15 Each of the ADCs is driven by a unique phase of clock f_D . Thus, each of the ADCs will sample a different input symbol. This operation is analogous to a time-division demultiplexing operation on the input stream.

Since the outputs of the ADCs are out of phase with respect to one another, a retiming circuit 98 is used to, in effect, align the signals to provide sixteen samples during each clock cycle of f_C to a set of parallel forward equalizers 100.

20 The forward equalizers 100 provide phase equalization (all-pass response) that equalizes, to some degree, the non-minimum-phase fiber response. Figure 6 depicts a portion (to reduce the complexity of the figure) of one embodiment of a parallel forward equalizer, specially, four parallel 4-tap finite impulse response (FIR) filters. Here, $y(n) = a_0x(n) + a_1x(n-1) + a_2x(n-2) + a_3x(n-3)$.

25 It will be understood that for a different number of inputs, the FIR filter of Figure 6 will be expanded to accept that number of inputs and provide that number of outputs. The FIR filter also will be expanded with respect to the number of filter taps. For example, in the embodiment of Figure 5, the FIR filter has sixteen inputs, sixteen outputs and sixteen filter taps. It should be appreciated, however, that the number of filter taps will not always equal the number of parallel blocks as is the case in this example.

30 The outputs of the forward equalizers 100 drive a 4-way interleaved, 4-dimensional trellis decoder 102. In a preferred embodiment the trellis decoder is a Viterbi decoder. As indicated in Figure 5, the Viterbi decoders for this example operate at a clock speed of 312.5 MHz. Significantly, the use of precoding in this embodiment simplifies the implementation of the Viterbi decoder because the Viterbi decoder does not need to be designed to handle intersymbol interference. Thus, the decoder does not have to be combined with decision feedback equalization, even though the decoder speed is very high. Moreover, branch metrics can be pipelined. Thus, virtually all critical path issues in the Viterbi decoder are eliminated.

1 The outputs of the parallel trellis decoders 102 drive a physical coding sublayer 104. The physical coding sublayer 104 performs several operations that are complementary to those performed by the physical coding sublayer 60 of Figure 2. This may include, for example, bit manipulation, descrambling and demultiplexing.

5 After the physical coding sublayer 104, the signals are routed to a system interface 106 and then off of the chip to the media access controller 84.

 The parallel implementation of the precoder is relatively difficult due to the feedback loop. The invention is based, in part, on the realization that look-ahead techniques can be used to implement the precoder in a pipelined or parallel architecture. Figures 7 - 12 describe several
10 implementations for a parallel precoder. These examples use a filter length, N , of 30 and a level of parallelism, L , of 16. In general, the number of filter taps that are needed depends on the characteristics of the channel (e.g., the fiber). For example, the length of the impulse response of the fiber determines the number of coefficients that are needed which, in turn, defines the number of taps.

15 Figure 7 is a simplified block diagram of a low latency parallel precoder incorporating overlapped block precoding. This embodiment is for a 32 wide precoder. That is, it provides 32 levels of parallelism. To reduce the complexity of Figure 7 only a few representative precoders and associated inputs and outputs have been illustrated.

 In effect, this embodiment provides the feedback data for a precoder via a set of parallel
20 precoders that operate on a series of earlier input states. For example, the input signal 110 for precoder 112 comprises information for input states x_{-1} through x_{-100} via decoders 114 and 116 and the intervening decoders that are not shown and their associate inputs (e.g., x_{-99} and x_{-100} and the other inputs that are not shown).

 It has been observed that good results may be obtained when the amount of overlap is
25 equal to approximately three times the number of taps. Thus, for this embodiment (32 taps), a length of overlap for each precoder has been selected to be 100. The amount of overlap may be characterized as the number of samples that are necessary for the transient response of the filter to reach a sufficiently low level such that the filter closely approximates an ideal filter with an infinite number input samples. The transient response depends on the parameters of the filter,
30 e.g., the closeness of the poles to the unit circle in the frequency domain. In practice the precise amount of overlap for a given system may be selected based on the characteristics (e.g., S/N) that are desired in the communication system.

 The embodiment of Figure 7 provides a relatively low latency of 32 clock cycles. However, it does require a relatively large number of precoders (132) with their associated
35 multipliers ($132 \times 30 = 3960$, for 32 outputs).

 Figure 8 is a conceptual block diagram for another embodiment of a parallel precoder. The input stream is divided into sixteen overlapping blocks. In this example, the block length is selected as 1000 and the overlap 120 between each block is equal to $3N$, which has been

1 rounded up to 100. The overlap 120 provides the necessary inputs from previous states for those
samples near a block boundary. Each block is filtered independently, and the first 100 outputs
are discarded. Thus processing overhead is increased by 10%. The sizes of the blocks are
5 selected to enable each block to, in effect, operate independently of the other blocks. In this way
one can define a filter response that is as close to the desired optimal response as is practical.

Referring to Figure 9, the embodiment of Figure 8 is implemented by routing the input to
sixteen buffers 124. For example, buffer 0 may store the 1000 bits for block 0, buffer 1 may store
the 1000 bits for block 1 and so forth. Each precoder then sequentially processes the bits in its
block of 1000 bits and outputs its results to an associated buffer 128. The outputs of the buffers
10 128 are multiplexed to form the precoded data.

To reduce the complexity of Figures 8 and 9 only a few representative blocks, buffers and
precoders have been illustrated.

This embodiment has the advantage that only sixteen precoders are needed and,
consequently, 480 multipliers (16×30). However, the buffers must operate at 5 GHz and
15 additional circuitry is required to provide the buffers.

Figure 10 is a simplified block diagram of another embodiment of a parallel precoder
comprising a double row precoder. To reduce the complexity of Figure 10 only a few
representative precoders and associated inputs and outputs have been illustrated.

In this embodiment, each precoder operates on 100 symbols in, for example, a serial
20 manner. All but one of the precoders in the lower row receives an input associated with 100
preceding inputs from an associated precoder in the top row.

For the example where there are 16 parallel precoders, 1600 outputs are computed in 100
clock cycles. This embodiment has the advantage that the hardware overhead is only increased
by a factor of two. However, the latency is longer (100 clock cycles in this example) and buffers
25 are needed to buffer the data for the 100 clock cycles.

Figure 11 is a simplified block diagram of another embodiment of a parallel precoder
comprising an overlapped double row precoder. To reduce the complexity of Figure 11 only a
few representative precoders and associated inputs and outputs have been illustrated.

In this embodiment there is an overlap of 32 samples between the precoders in the top
30 row. The latency is only 32 clock cycles. However, buffers are needed.

The lower row of precoders can be operated at a clock speed that is approximately four
times slower than the clock speed of the top row of precoders. This is because the precoders in
the top row operate on 132 samples while the precoders in the bottom row operate on 32 samples.
Thus, folding (time multiplexing) can be exploited to optimize the circuit.

35 Figure 12 is a simplified block diagram of another embodiment of a basic parallel precoder
comprising two parallel stages of a 3-tap infinite impulse response (IIR) filter. The circuit may
be described by the following equations:

$$\begin{aligned}
 1 \quad & y(n) = a_1 y(n-1) + a_2 y(n-2) + a_3 y(n-3) + x(n) \quad \text{EQUATION 1} \\
 & y(n) = a_1 [y(n-2) + a_2 y(n-3) + a_3 y(n-4) + x(n-1)] + \\
 & \quad a_2 y(n-2) + a_3 y(n-3) + x(n) \\
 & = (a_1^2 + a_2) y(n-2) + (a_1 a_2 + a_3) y(n-3) + a_1 a_3 y(n-4) + a_1 x(n-1) + x(n)
 \end{aligned}$$

$$5 \quad \text{EQUATION 2}$$

$n = 2k+2$ in equation (1) and $n = 2k+3$ in equation 2.

$$y(2k+2) = a_1 y(2k+1) + a_2 y(2k) + a_3 y(2k-1) + x(2k+2) \quad \text{EQUATION 3}$$

$$\begin{aligned}
 y(2k+3) = & a_1^2 + a_2 y(2k+1) + (a_1 a_2 + a_3) y(2k) + \\
 & a_1 a_3 y(2k-1) + a_1 x(2k+2) + x(2k+3) \quad \text{EQUATION 4}
 \end{aligned}$$

10 Extending this concept to an L-parallel implementation, $y(kL+L) \dots y(kL+2L-1)$ is computed in terms of $y(kL) \dots y(kL+L-1)$. In an L-parallel implementation, the clock speed is L times slower than the symbol speed, i.e., each delay element is L-times slower.

This basic implementation provides high speed and low latency. In addition, it is more stable because the poles are raised to the Lth power. Moreover, it has better finite precision effect. However, this implementation is suboptimal because it is difficult to minimize the power of the output. Hence, the embodiments of Figures 7 - 11 are preferred because these embodiment overcome this problem.

Referring now to Figure 13, one embodiment of a circuit that provides precoder initialization is described. In this embodiment, information related to the characteristics of the channel (e.g., precoder coefficients) are transmitted from the receive section of one transceiver to the transmit section of another transceiver over the channel. This initialization procedure takes place before the channel is completely operational.

During initialization a buffer captures a block of N samples (e.g., $N = 1024$) from the ADC at a 312.5 MHz clock rate. For example, in the receive section of the transceiver, the sixteen, 6 bit, 312.5 MHz signals from a retimer 140 (i.e., retiming 98 in Figure 5) are stored in a buffer 142.

Data from the buffer 142 is read out to provide the input for an auxiliary decision feedback equalizer. However, the forward equalizer 144 and decision feedback equalizer 146 are designed to operate at a reduced clock rate, for example, $F_{\text{SLOW}} = 100$ MHz, using the samples from the buffer 142.

While the buffer is being emptied, signal samples from the ADC are discarded. However, it will be appreciated that useful data can be transmitted and received during these blocks, except for a transient period at the beginning of the block. Since this procedure is executed at both ends of the link, this establishes a full-duplex channel with a data rate of approximately 200 Mbit/s (for $f_{\text{SLOW}} = 100$ MHz).

In one embodiment, this auxiliary channel may be used during startup to send, for example, decision feedback equalizer coefficients from the receiver to the transmitter thereby enabling programming of the precoder. For example, channel information generated by a

1 feedback filter 148 in the decision feedback equalizer 146 may be sent to framing logic 150 that
frames the channel information and, in cooperation with the transmitter 152, inserts it into the
channel for retrieval by the receiver on the other side of the channel. The framing operation
would include, for example, adding a marker to indicate the beginning of the channel
5 information.

Then when that channel information is received, a deframer 154 reads the output of the
decision feedback equalizer 146 to obtain the channel information. Here, the deframer 154
determines which input data is valid and locates the marker that identifies the beginning of the
channel information. The deframer 154 sends this channel information to its transmitter to
10 update the coefficients in the transmitter's precoder 156.

In another embodiment, the precoder 156 is continually adapted to the channel during
normal operation of the transceiver (e.g., when the channel is carrying data). In this case, a
portion of the bandwidth of the channel is allocated to carry the channel information.

In one embodiment the channel information consists of coefficients generated by an
15 adaptive equalization algorithm such as least mean square (lms). This information may be in the
form of 16-bit words. The framer and associated processing would serialize these 16-bit words
and route the serial bits to be sent over the channel. At the other end of the channel, the deframer
and associated processing use known characteristics of the coefficients to reassemble the
coefficients and program each coefficient in the appropriate manner in the precoder. In
20 accordance with the invention, other methods of generating channel information may be used as
well as other types of information that characterize the channel. In these embodiment, additional
processing may be needed to generate coefficients or other information for the precoder.

Referring now to Figures 14 - 19, one embodiment of an analog interface for the
transmission system will be treated in more detail. Figure 14 depicts a high level view of an
25 analog interface that may be used for a 10 Gbit/s Ethernet channel. The input to the DAC 160
in the transmit section consists of a signal with 8-bit resolution. In this case, a minimum of 6 bit
resolution is required for the ADC 162 in the receive section. Both the DAC 160 and the ADC
162 operate at a clock rate of 5 GHz. The receive high pass corner is 200 MHz. The receive
section also includes a -20 ... 0 dB attenuator for amplitude control.

30 Figure 15 depicts one embodiment of a receive ADC using, for example, eight (assuming
 $N = 8$) parallel interleaved ADCs 162. Each of the eight ADCs 162 generate 6 bit samples at a
sampling rate of $5 \text{ GHz}/8 = 625 \text{ MHz}$. Sample and hold circuits 166 are used to guarantee a low
jitter sampling. A clock 168 generates eight phases 168 of the sample clock, spaced at 200
picoseconds. In this way the ADCs 168 are effectively interleaved so that each ADC processes
35 a portion of the input signal. Gain and phase errors between the ADCs may be compensated for
digitally.

In some embodiments a demultiplexer may be used to widen the data bus from the ADCs
168. For example, again assuming $N = 8$, in the embodiment of Figure 15 eight 1:2 multiplexers

1 170 are used to convert the eight 625 MHz digital outputs of the ADCs 168 to sixteen 312.5 MHz signals.

In one embodiment, the ADCs are implemented in 0.15μ CMOS with a 1.8 V supply voltage, differential analog input of 1.0 Vpp, distortion at 2 GHz < -40 dB, a bit error rate of 10^{-15} , and clock jitter of < 1.5 picosecond rms.

Figure 16 depicts exemplary clock jitter requirements. V_{in} is defined as $A \sin \omega t$ (assuming a sine wave input signal). Maximum amplitude is assumed to be 1 LSB. And $\Delta t = \Delta A / (A \omega \cos \omega t)$ with $\Delta A = 2A/2^n$.

Then $\Delta t = 2^{-n} / \pi f_{in} \cos(2\pi f_{in} - t)$, where f_{in} = input frequency and n = the resolution of the ADC. The maximum at zero crossing of the input signal $\Delta t_{max} = 2^{-n} / \pi f_{in}$. Where $n = 6$ and $f_{in} = 1$ GHz, $\Delta t_{max} = 5$ picoseconds.

Figure 17 is a block diagram of one embodiment of a phase locked loop architecture with eight interleaved clocks operating at 625 MHz. A phase detector 172 compares the phase of the reference clock and a divide-by-N circuit 174. The output of the phase detector 172 is sent to a charge pump (Q pump) 186 and then a loop filter 176 to generate a control voltage for an LC-based voltage controlled oscillator 178. A divide-by-8 circuit 179 provides eight phases of a 625 MHz clock.

Figure 18 is a block diagram of one embodiment of an LC-based voltage controlled oscillator for a low jitter clock generator. Switched capacitors 180 are controlled by the state machine 182 (Figure 17) to adjust the VCO center frequency over process and temperature (+/- 20%). The varactor 184 is controlled by the charge pump 186 (Figure 17). This implementation utilizes a differential approach for power supply and substrate noise immunity.

Figure 19 is a block diagram of one embodiment of a DAC circuit and transmit optical interface. The input to the circuit is an 8-bit digital signal. The output is a 5 gigasample per second signal. In one embodiment, a current-mode DAC circuit converts precoded PAM-5 symbols to driver current.

Significantly, this embodiment uses parallel interleaved DACs and a multiplexer or summer to accomplish high speed digital to analog conversion. That is, the output signals from the four 1.25 GHz current mode DACs 185 are interleaved to provide a 5 gigasample per second output signal.

In a preferred embodiment the DACs and the multiplexers are implemented using 0.15μ CMOS. Representative characteristics of this preferred embodiment include: spurious-free dynamic range > 48 dB; total harmonic distortion > 48 dB; single-ended output current = 5 to 15 mA; and output capacitance < 5 pF.

In one embodiment the 125 GHz output signals from the DACs 185 are sent to a multiplexer 186. The multiplexer 186 time-multiplexes the four 125 GHz signals to generate a 5 GHz output signal under control of the clock signals generated by a clock circuit 187.

1 In another embodiment the 125 GHz output signals from the DACs 185 are sent to a summer 186. In this case, the outputs of the DACs are, in effect, tied together. Time-division multiplexing of the 125 GHz signals to produce a 5 GHz signal is accomplished in this case by carefully controlled timing of the clock signals to the DACs 195. For example, CLK0, CLK1, CLK2 and CLK3 may be phase shifted from one another so that, in effect, only one of the DACs 195 drives its output at a given time.

5 The output of the multiplexer 186 or the summer 186 drives a buffer 188. The function of the buffer is to isolate the capacitive output of the DAC circuit (e.g., DACs 185 and multiplexer/summer 186) from the series resistance of the laser diode 189. Typically, the interleaving of the DACs 185 results in a relatively high output capacitance for the DAC circuit. Thus, the buffer 188 reduces the bandlimiting effect that this relatively high output capacitance would have on the output signal.

10 In one embodiment, the buffer 188 is a current buffer. One embodiment of a current buffer is shown in Figure 19. The NPN transistors Q1 and Q2 may, for example, be silicon germanium RF transistors made with 70 GHz ft SiGe process. One example of a suitable transistor is the Infineon BFP620 transistor.

15 An example operating point for the current buffer of Figure 19 is: I_{diode_DC} = approximately 10 mA; input impedance < 4.0 ohms; input capacitance < 0.9 pF; and output capacitance < 0.15 pF.

20 Typically the optical output device is a laser diode 189 as depicted in Figure 19. For example, a vertical cavity surface emitting laser (VCSEL) may be used. In one embodiment the operating characteristics of the laser diode may be: I_{on_max} = 5 mA; input capacitance < 0.8 pF; and series resistance < 30 ohms.

25 The specific implementation of a DAC circuit and a transmit optical interface according to the invention may take many forms. For example, the number, format and speed of the input signals, the number of DACs, the operating speed and characteristics of the components and the speed of the output signal depend on system design requirements.

30 Moreover, different types of DACs, multiplexers, summers, buffers and optical output devices may be used to implement a DAC circuit and transmit optical interface according to the invention. For example, many of these components may be implemented in silicon germanium. The multiplexer 186 may be implemented in a separate integrated circuit than the DACs 185. The DACs 185 may be implemented in a different integrated circuit than the rest of the transmitter. Different circuits may be used for the current buffer. The buffer 188 may be a voltage buffer instead of a current buffer.

35 In practice, the number of ADCs, DACs, clock signals and the respective operating speed of each of the components described above in conjunction with Figures 14 - 19 will depend, for example, on the number of parallel levels of these and other components in the system as well

1 as on the desired operating speed of these components and the data rates of the input and output signals.

5 Figure 20 is a block diagram of one embodiment where transceivers implementing the teachings of the invention are used to transmit electrical signals between circuit boards 190 over a backplane 192. In this embodiment, coded PAM-5 signals are driven over electrical paths 191 in the backplane 192 by electrical interfaces 193. It should be understood that, in general, the primary difference between the circuit of Figure 20 and the other circuits described herein is the use of an electrical interface rather than an optical interface (as shown in Figure 1). Thus, the embodiment of Figure 20 may include, for example, parallel precoding and/or other techniques as described and taught herein in accordance with the invention. Typically, the length of the electrical path in this implementation would be limited to a distance of approximately 30 inches.

10 Figure 21 is a block diagram of an embodiment where transceivers implementing parallel precoding according to the teachings of the invention are used to transmit electrical signals between router switches 194 via at least one coaxial or twinaxial cable 196. This embodiment is similar to the one described in conjunction with Figure 20 except that the electrical interface (not shown) may be particularly adapted to drive coaxial cable or twinaxial cable. Typically the length of the cable 196 in this implementation with PAM-5 signals operating at 5 GHz would be limited to a distance of approximately 10 -15 meters.

15 Figure 22 is a block diagram of one embodiment where transceivers 198 implementing precoding according to the teachings of the invention are incorporated into an optical module 200 with DACs 202, ADCs 204 and optoelectronics 206. The optoelectronics used for a transceiver typically incorporates a laser photodetector, a laser driver and amplifiers including a trans-impedance amplifier.

20 The teaching of the invention may be incorporated into a wide variety of implementations. For example, many of the components described herein may or may not be used in a given implementation. One embodiment of a system constructed according to the invention does not use trellis decoding or trellis decoding. In this case, in the transmitter the uncoded digital signals may be input to the parallel Tomlinson precoders. In the receiver the digital output of the forward equalizers may be passed directly to the physical coding sublayer. This embodiment may be used to reduce system cost and/or power dissipation. However, in general, a system without trellis decoding will have a higher bit error rate. In addition, such a system typically would be operated with a channel with a higher signal-to-noise ratio (S/N).

25 Another embodiment of a system constructed according to the invention uses the forward equalizers, but not the transmit equalization. In general, this system typically would be used in relatively low noise environments because noise may be amplified to a greater extent by the forward equalizers. In this case, in the receiver the output of the ADC section may pass directly to the trellis decoder (if trellis coding is used) or, in some embodiments, to other digital signal processing operations.

1 Another embodiment of a system constructed according to the invention does not use a forward equalizer. In this case, all equalization may be performed in the precoder or in a decision feedback equalizer. Typically this embodiment may be used when the communications system has little or no intersymbol interference.

5 Another embodiment of a system constructed according to the invention does not use Tomlinson-Harashima precoding. For example, some systems do not provide equalization.

An example of a system that may not incorporate equalization will be described below in conjunction with the simplified block diagram of Figure 23. Figure 23 illustrates, in part, that a variety of processing tasks may be performed by a system designed in accordance with the invention. To this end, a transmitter 210 and a receiver 220 are shown as including one or more processing elements 212 and 224, respectively. In some embodiments these processing elements may be implemented in parallel.

10 The processing elements 212 typically comprise circuitry that performs processing functions, for example, a digital signal processor. A transmit-side processing element 212 may comprise, for example, a transmit equalizer such as a pre-emphasis filter, a Tomlinson-Harashima precoder and/or a dynamics limited precoder. In some embodiments, a processing element 212 may comprise, for example, a trellis encoder, a convolutional encoder, or a block encoder.

15 The receive-side processing elements 224 typically comprise circuitry that performs processing functions, for example, a digital signal processor. A processing element 224 may comprise, for example, a crosstalk canceller, a forward equalizer and/or a decision feedback equalizer. In some embodiments, a processing element 224 may comprise, for example, a trellis decoder, a convolutional code decoder, or a block code decoder. In other embodiments, the processing elements 224 are not incorporated into the design.

20 In one implementation of the embodiment of Figure 23, digital input signals 208 to the transmitter 210 are processed by one or more processing elements 212. In other embodiments, the processing elements 212 are not incorporated into the design. In the latter case, the transmitter typically would not perform coding or equalization operations.

25 If a processing element is incorporated into the design, the output of a processing element 212 is eventually sent to a DAC 214 which may be implemented, for example, as described herein. The output of a DAC 214 (or the multiplexed outputs of the DACs 214 in the case of parallel DACs 214) is sent over a channel via optical or electrical interfaces 216 and 218 to the receiver 220. One or more ADCs 222 in the receiver 220 convert the analog signal to digital signals, for example, as discussed herein, to perhaps be processed by one or more processing elements 224 and/or one or more symbol-by-symbol decoders 226.

30 In some embodiments, the processing elements 224 are not incorporated into the design. In this case, the receiver may not perform decoding or equalization operations.

1 If the symbol-by-symbol decoder 226 is incorporated into the design, it may be
implemented as a relatively simple threshold detection device that compares the input signal with
threshold levels to determine, for example, the PAM level of the received signal (e.g., -2, -1, 0,
1, 2). The symbol-by-symbol decoder functions may be implemented by a digital signal
5 processor.

 In view of the above, it may be seen that the use of precoding may provide several
advantages over receiver equalization. A parallel precoder is, in general, easier to implement
than a parallel decision feedback equalizer in the receive section. When using trellis coded
modulation, precoding simplifies the implementation of the trellis decoder because the trellis
10 decoder does not need to resolve the effects of intersymbol interference. Precoding avoids error
propagation, which may be a problem in decision feedback equalizers. Moreover, the techniques
described herein provide an asymptotically optimal architecture in that the combination of
precoding with coded modulation approaches the Shannon bound for channel capacity when good
modulation codes are used.

15 The illustrative systems described herein may be implemented in a variety of ways. For
example the transmitter and receiver sections 50 and 82 typically would be implemented as a
CMOS PHY transceiver integrated circuit. This implementation may provide very good
performance at a relatively low cost. It should be appreciated, however, that these circuits may
be implemented on separate integrated circuits. For example, the transmitter and receiver
20 sections may be implemented on separate chips. The DACs and ADCs may be implemented on
chips apart from the other components of the transmitter and receiver. In addition, the transmitter
and receiver or some of their components may be implemented using different integrated circuit
technology. For example, the DACs and ADCs may be implemented as silicon germanium
devices.

25 The chip interfaces (e.g., buses 28 and 32 in Figure 1) may take a variety of different
forms. In one embodiment the interfaces between the transmitter 50 and the media access
controller 52 (Figure 2) and between the receiver 82 and the media access controller 85 (Figure
5) consist of XAUI interfaces. In another embodiment the chip interfaces may comprise X-GMII
interfaces. It should be understood, however, that the type of the chip interface will depend on
30 the particular application in which the chip will be used. For example, different interfaces may
be specified for different data rates, different bus architectures and so forth.

 As described above, the teaching of the invention can be applied to both optical and non-
optical channels (e.g., electrical and wireless channels). Optical channels include, for example,
single mode fiber and multimode fiber. In particular the embodiment described in conjunction
35 with Figures 1 - 6 can operate over existing multimode fiber installations up to distances of at
least 300 meters. The system can operate with single channel optoelectronics. That is, a single
laser and a single photodetector. Significantly, the invention provides an especially attractive

1 system for transmitting high speed data over multimode fiber because these equalization techniques effectively compensate for the bandwidth limitations of this type of fiber.

The parallel processing techniques according to the invention may be implemented in many different ways as well. For example, the number of parallel convolutional
5 encoder/decoders, block encoders/decoders, trellis encoders/decoders, Tomlinson-Harashima precoders, DACs, ADCs, forward equalizers, digital signal processor elements and symbol-by-symbol decoders used in a given implementation will depend on system design requirements. Similarly the speed at which these circuits operate will depend on the number of parallel levels and the speed of the transceiver input and output signals. In general, typical design requirements
10 include the speed of the input signal, the speed of the integrated circuit technology, the maximum power dissipation and the desired cost of the integrated circuit.

In many embodiments the main processing elements treated herein such as the parallel convolutional encoder/decoders, block encoders/decoders, pre-emphasis filters, decision feedback equalizers, trellis encoders/decoders, Tomlinson-Harashima precoders, forward
15 equalizers, digital signal processor elements and symbol-by-symbol decoders may be implemented as separate digital signal processor elements on an integrated circuit. Depending on system design requirements, as discussed herein a system constructed according to the invention may incorporate parallel implementations of some or all of the these digital signal processors.

20 The invention may be practiced with different data modulation schemes. Including, for example, any level of PAM coding (e.g., PAM-3, PAM-7).

A variety of components may be used to implement the electrical-optical interfaces (e.g., optical interfaces 40 and 42 in Figure 1). These interfaces may include lasers and photodetectors and other types of optical transmitters and optical receivers.

25 Also, the invention may be practiced with a wide variety of encoding and decoding schemes. Including different trellis encoding schemes and convolutional encoding and block encoding.

In summary, the invention described herein provides an effective communications system using equalization precoding. While certain exemplary embodiments have been described in
30 detail and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive of the broad invention. It will thus be recognized that various modifications may be made to the illustrated and other embodiments of the invention described above, without departing from the broad inventive scope thereof. In view of the above it will be understood that the invention is not limited to the particular embodiments or
35 arrangements disclosed, but is rather intended to cover any changes, adaptations or modifications which are within the scope and spirit of the invention as defined by the appended claims.

1 WHAT IS CLAIMED IS:

1. A integrated circuit transceiver comprising:
at least one transmit section comprising at least one parallel equalization precoder;
5 and
at least one receive section comprising at least one parallel equalization decoder.
2. An optical transmission system comprising:
at least one equalization precoder for generating a precoded signal;
10 at least one optical driver for converting the precoded signal to an optical signal and adapted to transmit the precoded signal over an optical channel;
at least one optical receiver adapted to receive the optical signal from the optical channel and for converting the optical signal to an electrical signal; and
at least one equalization decoder for decoding the electrical signal.
15
3. A system for initializing an equalization precoder comprising:
at least one buffer for receiving data from a transmitter via a channel;
at least one decision feedback equalizer adapted to receive data from the at least one buffer and adapted to generate channel data associated with a response of the channel;
20 and
at least one data inserter for inserting at least a portion of the channel data into the channel for transmission to a precoder in the transmitter.
- 25 4. A method for providing equalization precoding comprising the steps of:
performing trellis encoding on an input data signal to generate trellis encoded data;
performing equalization precoding on the trellis encoded data to generate precoded data;
performing forward equalization on received encoded data to generate forward
30 equalized data; and
performing trellis decoding on the forward equalized data to generate decoded data.
5. A transceiver comprising:
at least one receiver comprising:
35 at least one interleaved analog to digital converter.
6. The transceiver of claim 5 wherein the receiver further comprises parallel digital signal processors.

- 1 7. The transceiver of claim 5 wherein the receiver further comprises at least one digital signal processor comprising at least one forward equalizer.
- 5 8. The transceiver of claim 5 wherein the receiver further comprises at least one digital signal processor comprising at least one crosstalk canceller.
9. The transceiver of claim 5 wherein the receiver further comprises at least one digital signal processor comprising at least one trellis decoder.
- 10 10. The transceiver of claim 5 wherein the receiver further comprises at least one digital signal processor comprising at least one symbol by symbol decoder.
11. The transceiver of claim 5 wherein the receiver further comprises at least one digital signal processor comprising at least one decision feedback equalizer.
- 15 12. The transceiver of claim 5 wherein the receiver further comprises at least one digital signal processor comprising at least one convolutional code decoder.
13. The transceiver of claim 5 wherein the receiver further comprises at least one digital signal processor comprising at least one block code decoder.
- 20 14. A transceiver comprising:
at least one transmitter comprising:
at least one interleaved digital to analog converter.
- 25 15. The transceiver of claim 14 wherein the transmitter further comprises parallel digital signal processors.
16. The transceiver of claim 14 wherein the transmitter further comprises at least one digital signal processor comprising at least one transmit equalizer.
- 30 17. The transceiver of claim 16 wherein the at least one transmit equalizer comprises at least one Tomlinson-Harashima precoder.
- 35 18. The transceiver of claim 16 wherein the at least one transmit equalizer comprises at least one dynamics limited precoder.

- 1 19. The transceiver of claim 14 wherein the transmitter further comprises at least one digital
signal processor comprising at least one trellis encoder.
- 5 20. The transceiver of claim 14 wherein the transmitter further comprises at least one digital
signal processor comprising at least one convolutional encoder.
21. The transceiver of claim 14 wherein the transmitter further comprises at least one digital
signal processor comprising at least one block encoder.
- 10 22. An optical transmission system comprising:
at least one receiver comprising:
at least one electrical-optical interface; and
at least one interleaved analog to digital converter.
- 15 23. The optical transmission system of claim 22 wherein the receiver further comprises
parallel digital signal processors.
24. The optical transmission system of claim 22 wherein the receiver further comprises at least
one digital signal processor comprising at least one forward equalizer.
- 20 25. The optical transmission system of claim 22 wherein the receiver further comprises at least
one digital signal processor comprising at least one crosstalk canceller.
26. The optical transmission system of claim 22 wherein the receiver further comprises at least
25 one digital signal processor comprising at least one trellis decoder.
27. The optical transmission system of claim 22 wherein the receiver further comprises at least
one digital signal processor comprising at least one symbol by symbol decoder.
- 30 28. The optical transmission system of claim 22 wherein the receiver further comprises at least
one digital signal processor comprising at least one decision feedback equalizer.
29. The optical transmission system of claim 22 wherein the receiver further comprises at least
one digital signal processor comprising at least one convolutional code decoder.
- 35 30. The optical transmission system of claim 22 wherein the receiver further comprises at least
one digital signal processor comprising at least one block code decoder.

- 1 31. A optical transmission system comprising:
at least one transmitter comprising:
at least one electrical-optical interface; and
at least one interleaved digital to analog converter.
- 5 32. The optical transmission system of claim 31 wherein the transmitter further comprises parallel digital signal processors.
- 10 33. The optical transmission system of claim 31 wherein the transmitter further comprises at least one digital signal processor comprising at least one transmit equalizer.
34. The optical transmission system of claim 33 wherein the at least one transmit equalizer comprises at least one Tomlinson-Harashima precoder.
- 15 35. The optical transmission system of claim 33 wherein the at least one transmit equalizer comprises at least one dynamics limited precoder.
36. The optical transmission system of claim 31 wherein the transmitter further comprises at least one digital signal processor comprising at least one trellis encoder.
- 20 37. The optical transmission system of claim 31 wherein the transmitter further comprises at least one digital signal processor comprising at least one convolutional encoder.
38. The optical transmission system of claim 31 wherein the transmitter further comprises at least one digital signal processor comprising at least one block encoder.
- 25
- 30
- 35

1/23

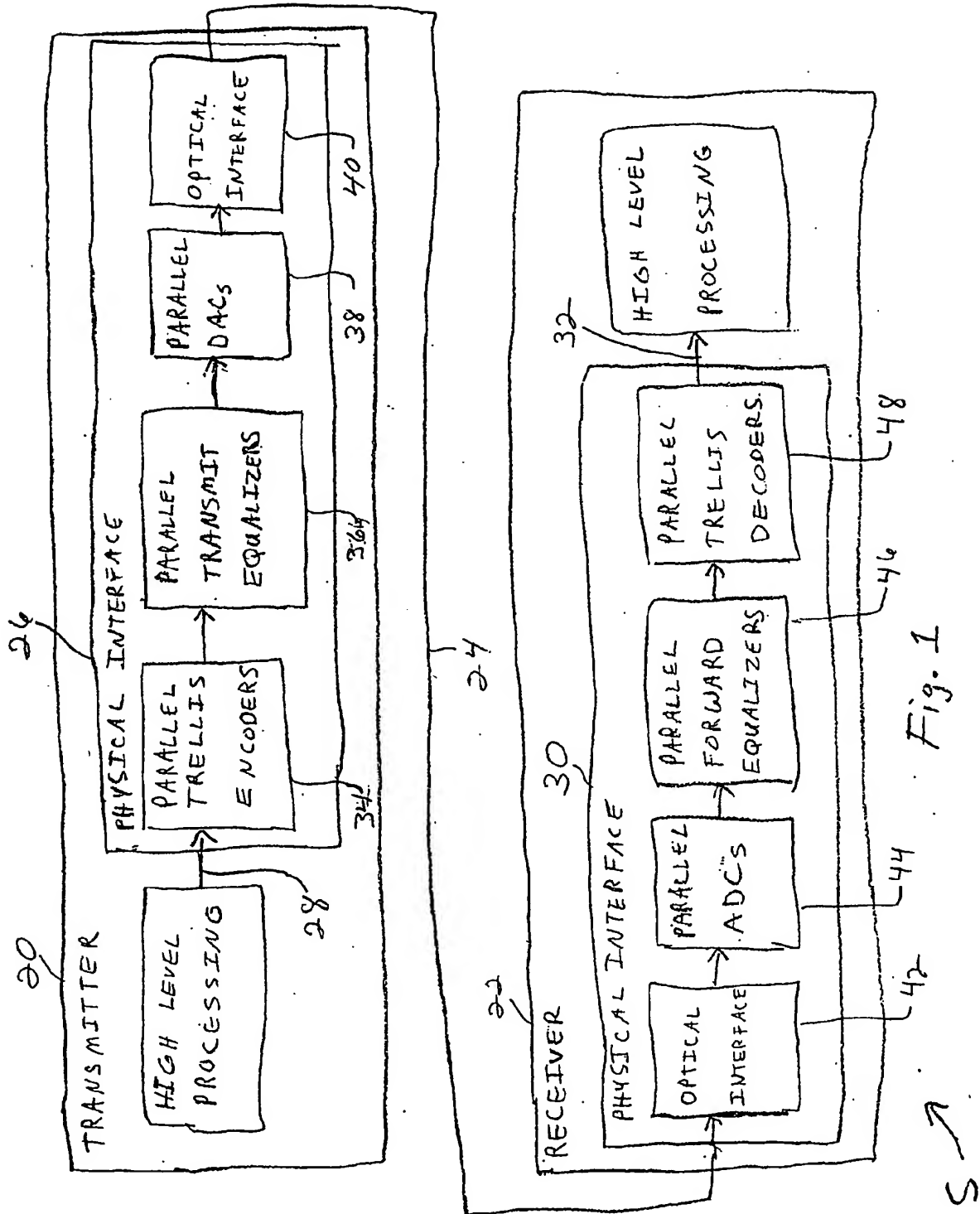


Fig. 1

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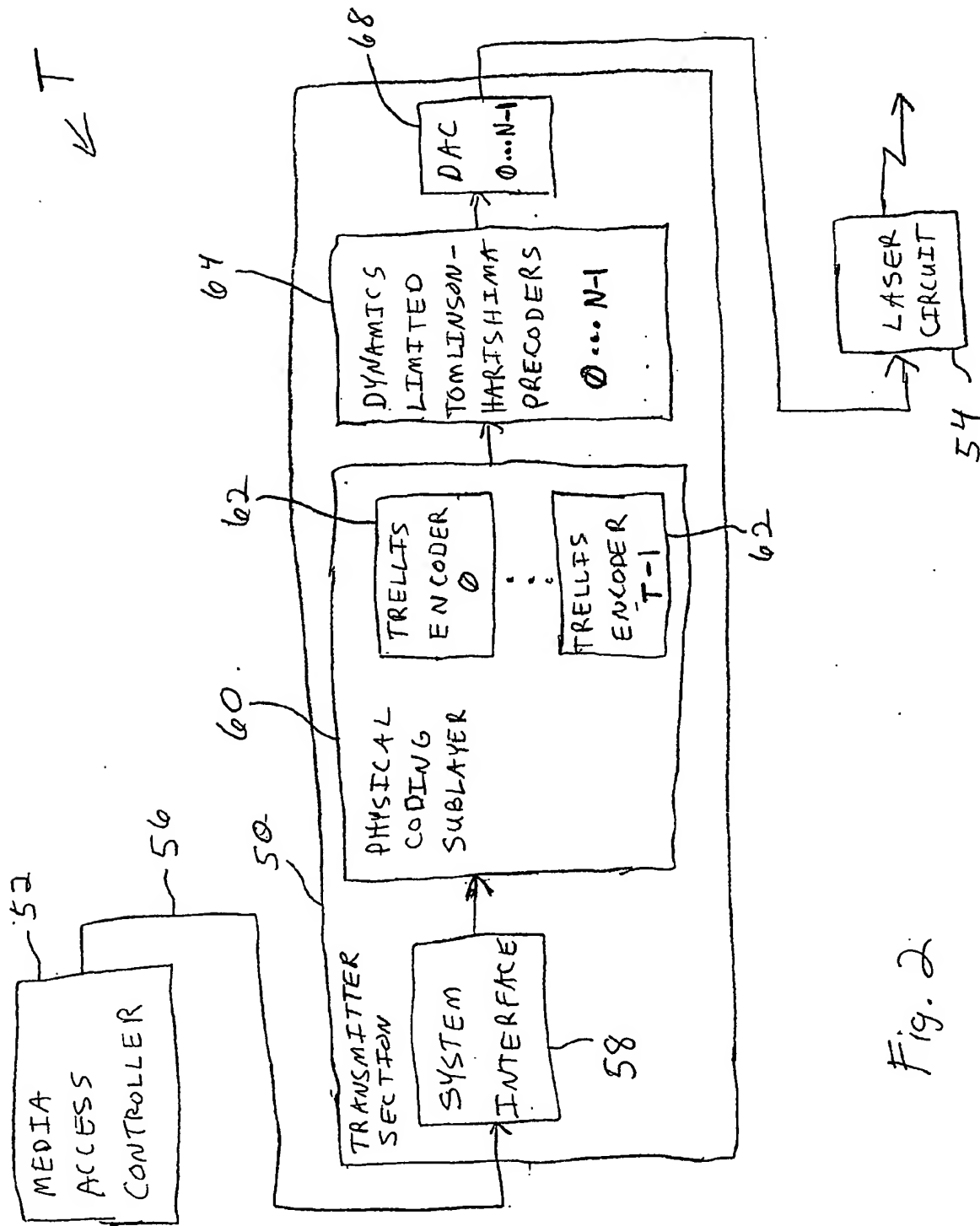


Fig. 2

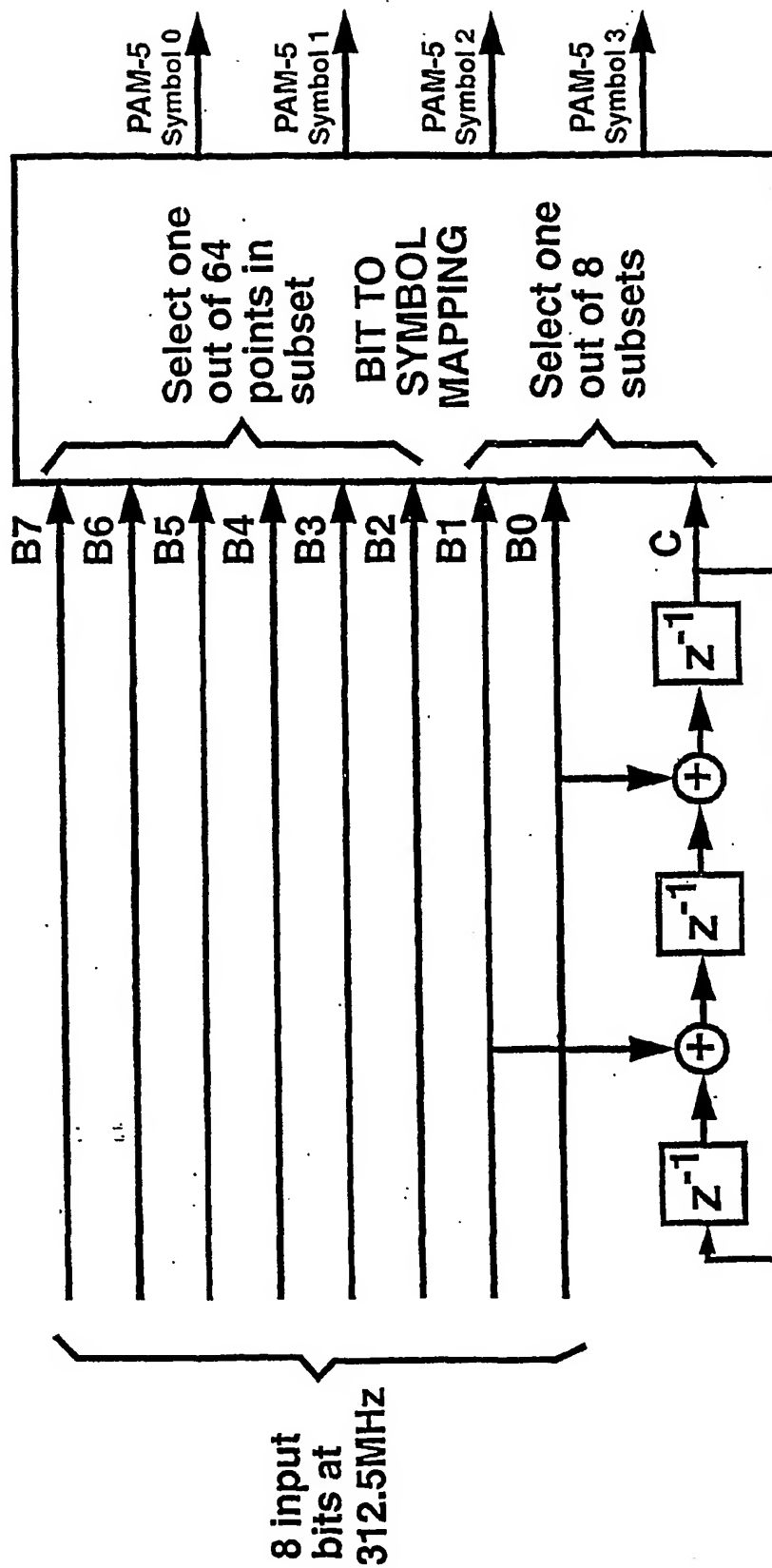


Fig. 3

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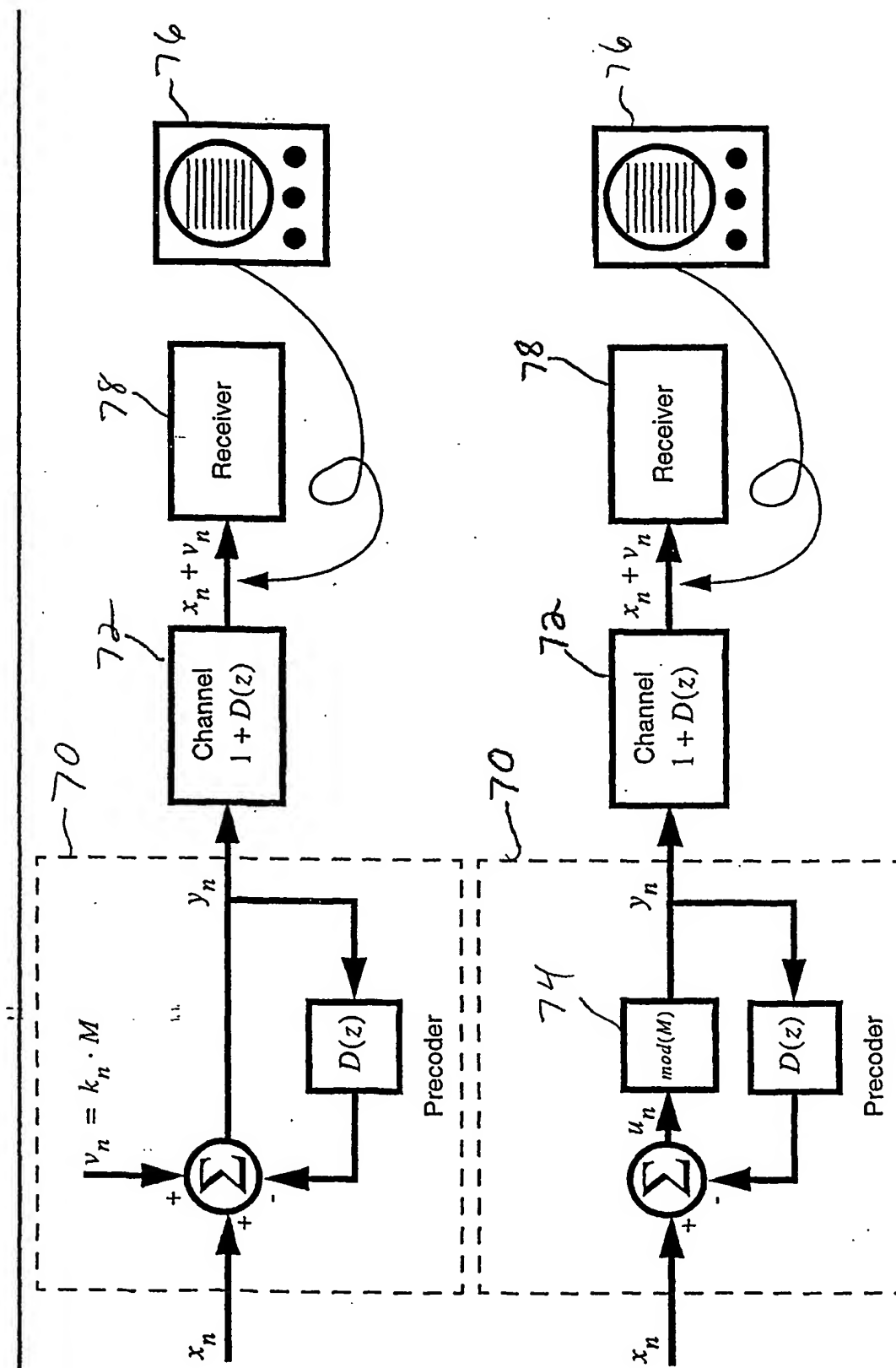


Fig. 4

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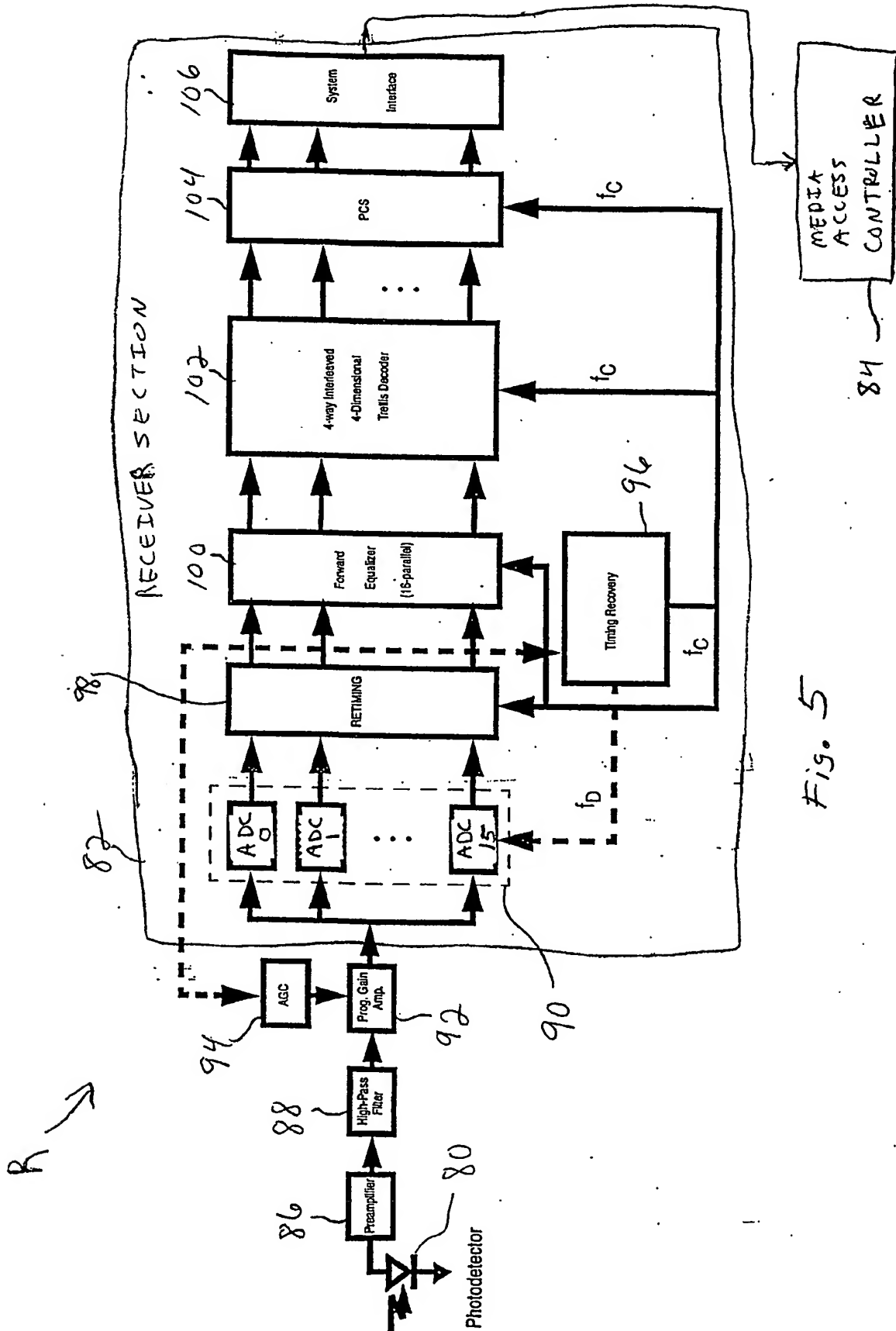


Fig. 5

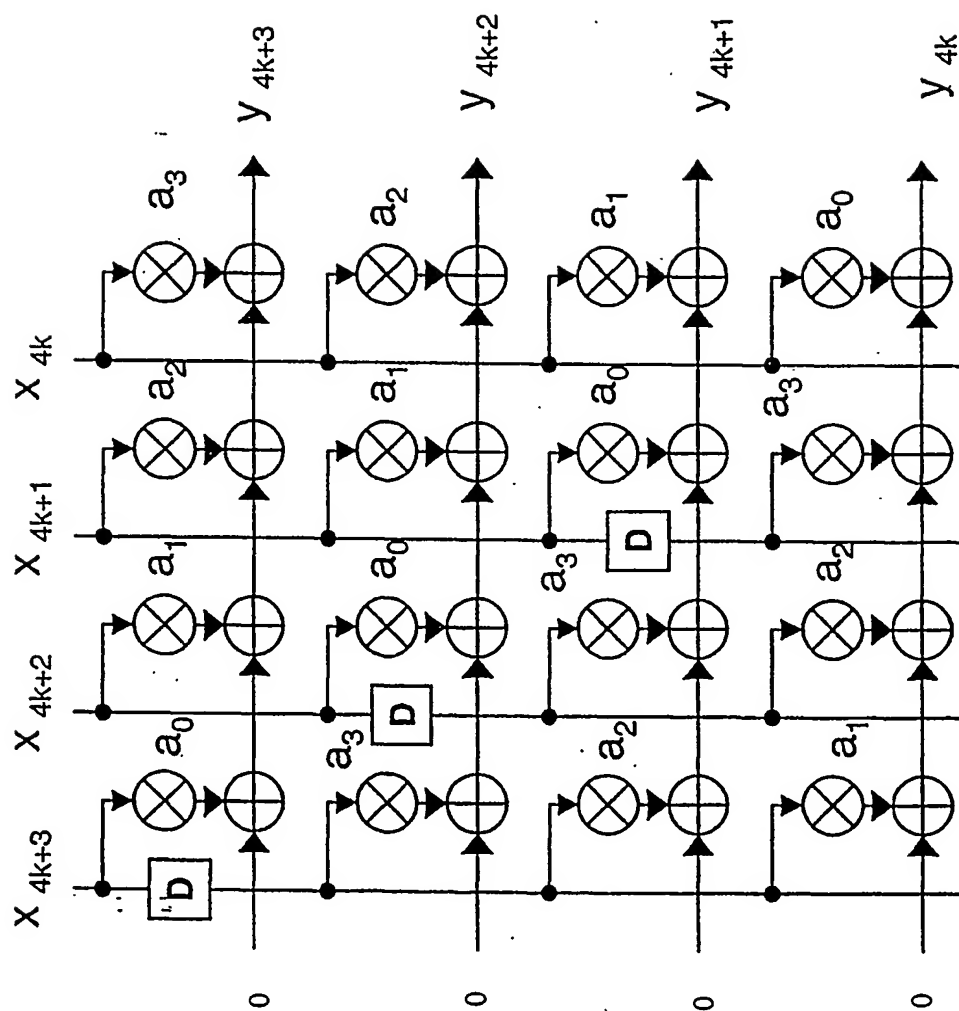
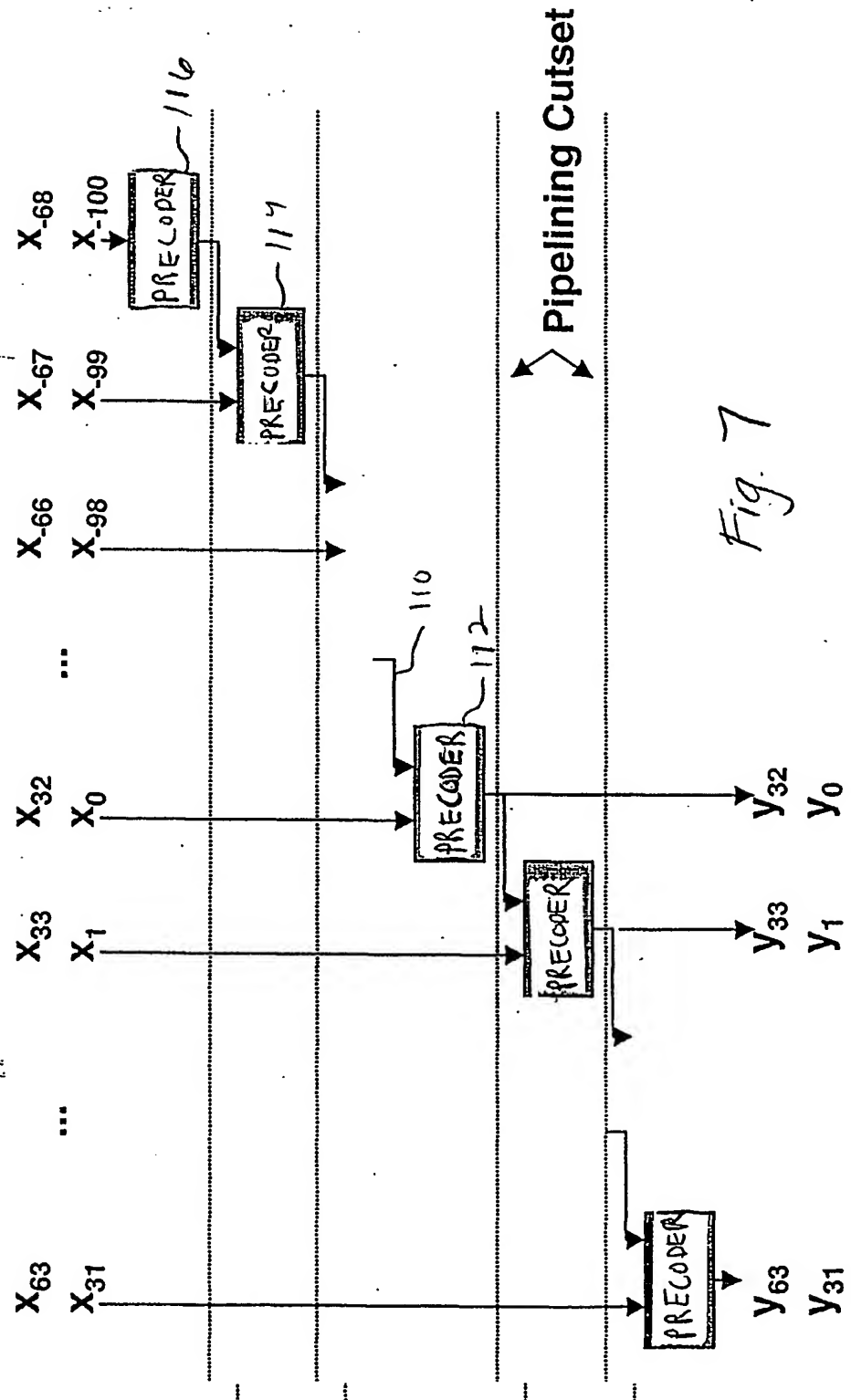


Fig. 6



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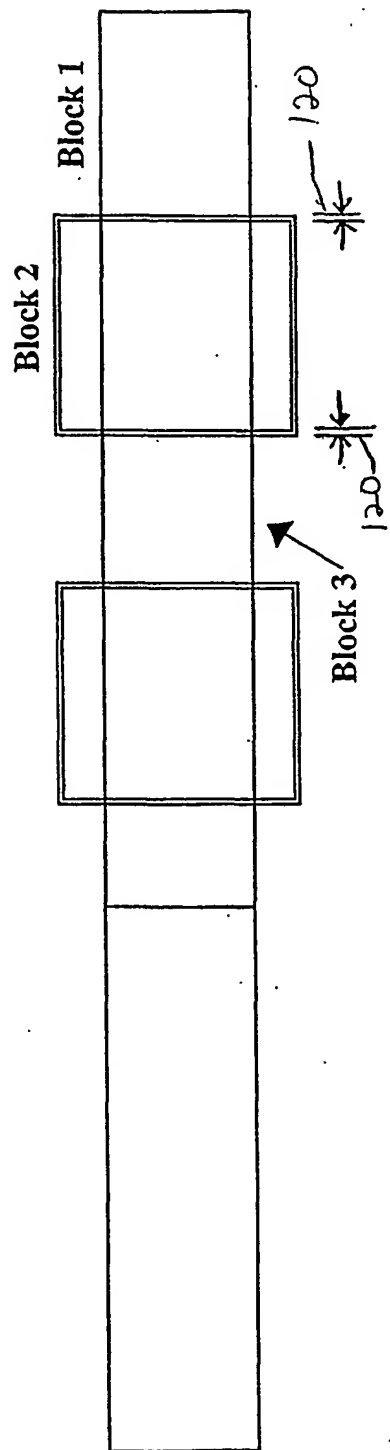


Fig. 8

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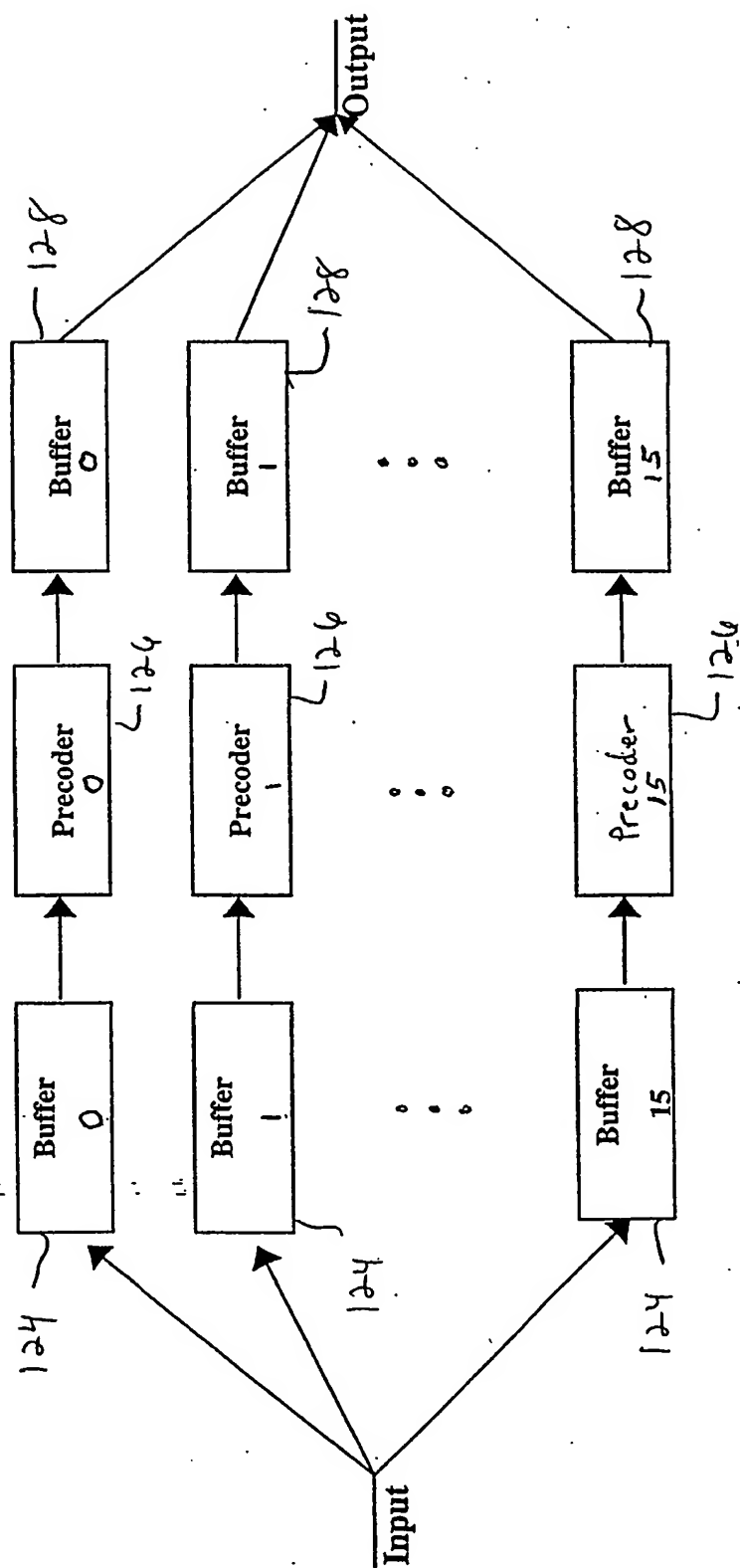


Fig. 9

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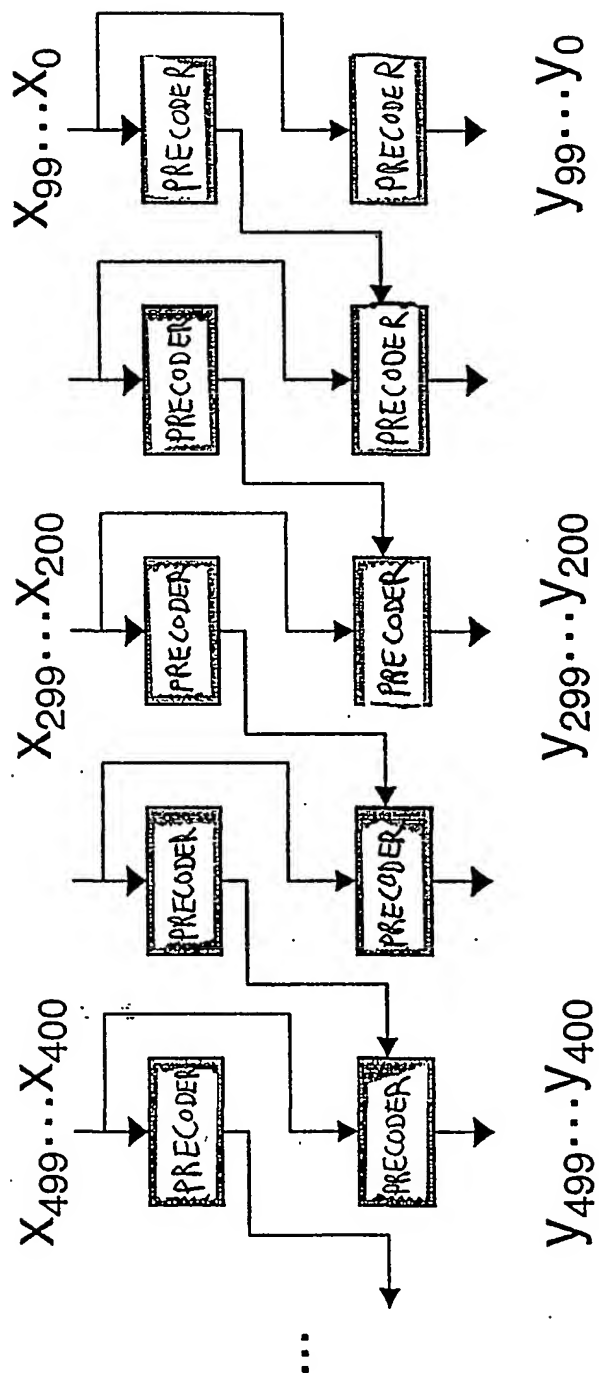


Fig. 10

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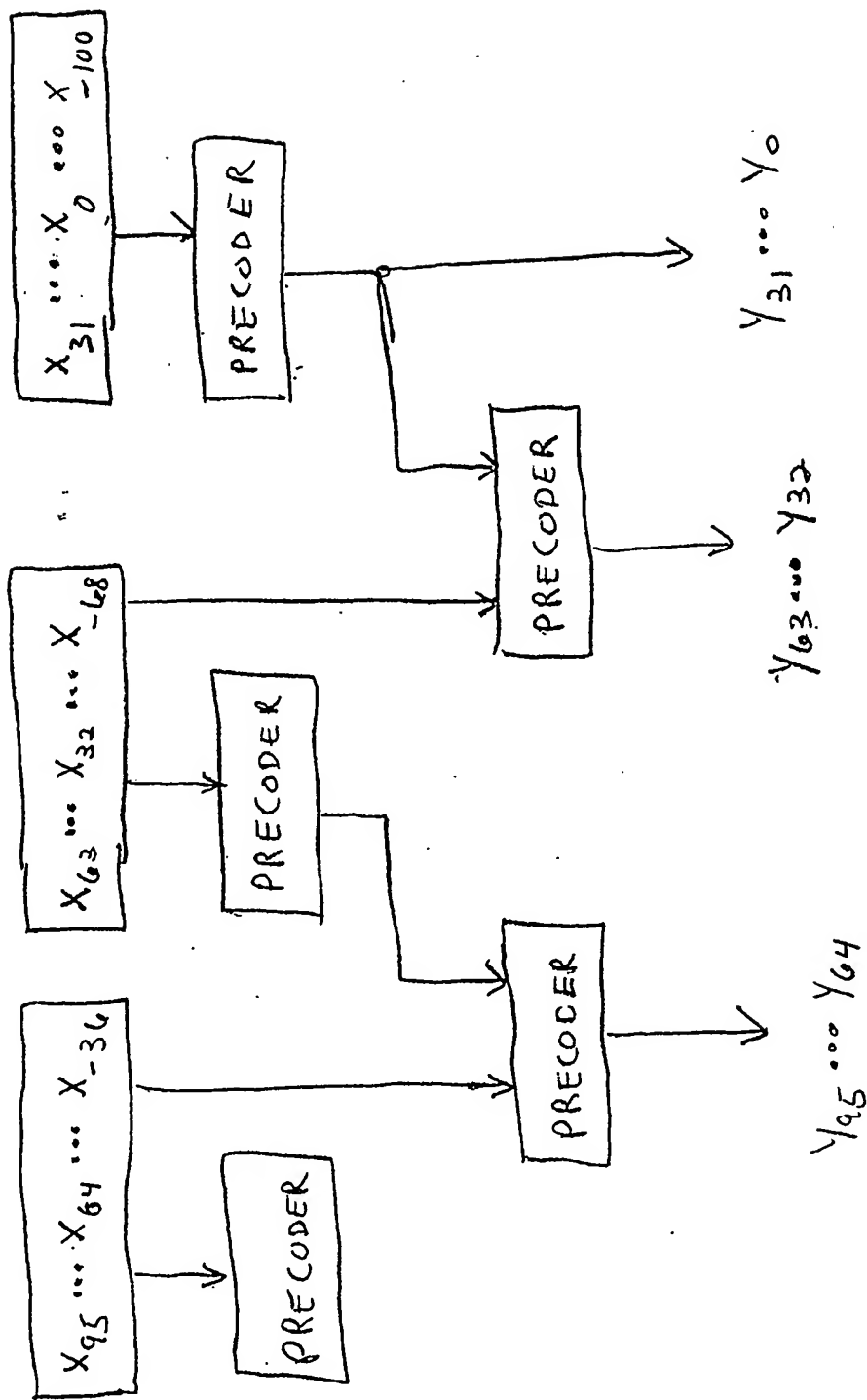


Fig. 1A

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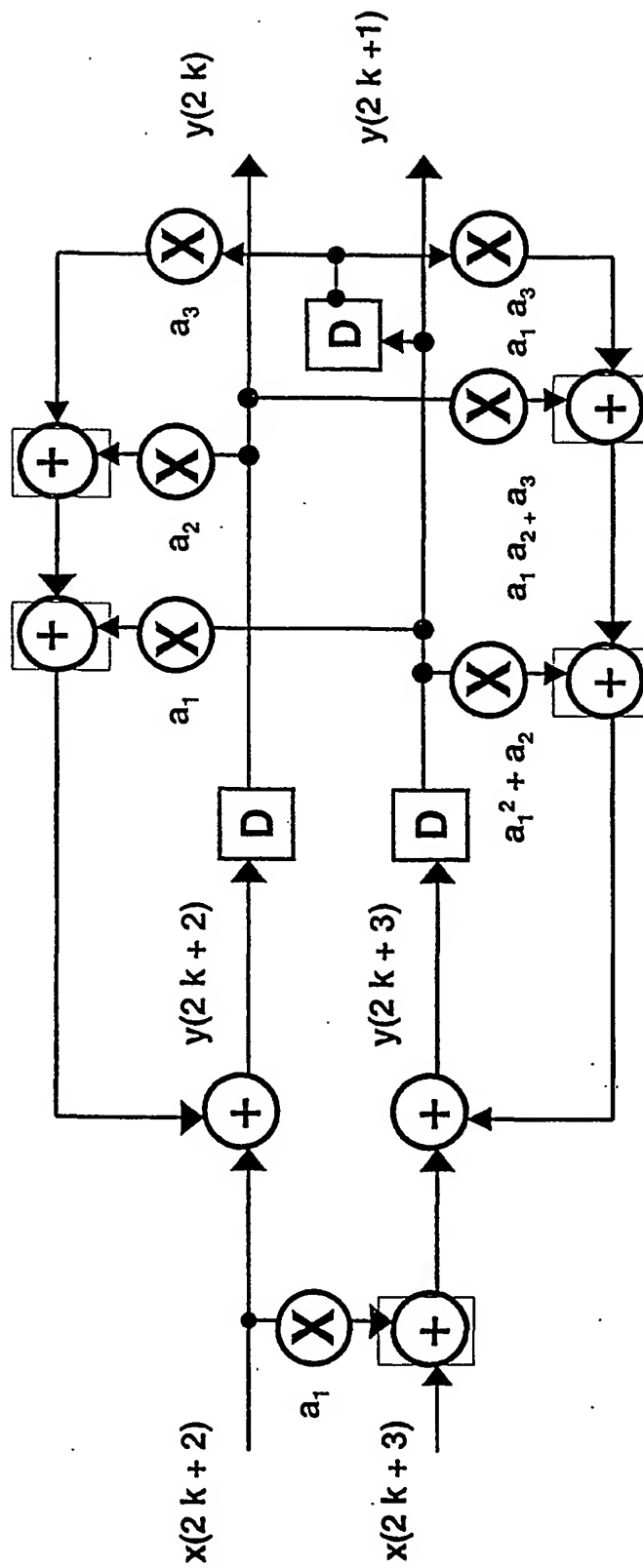


Fig. 12

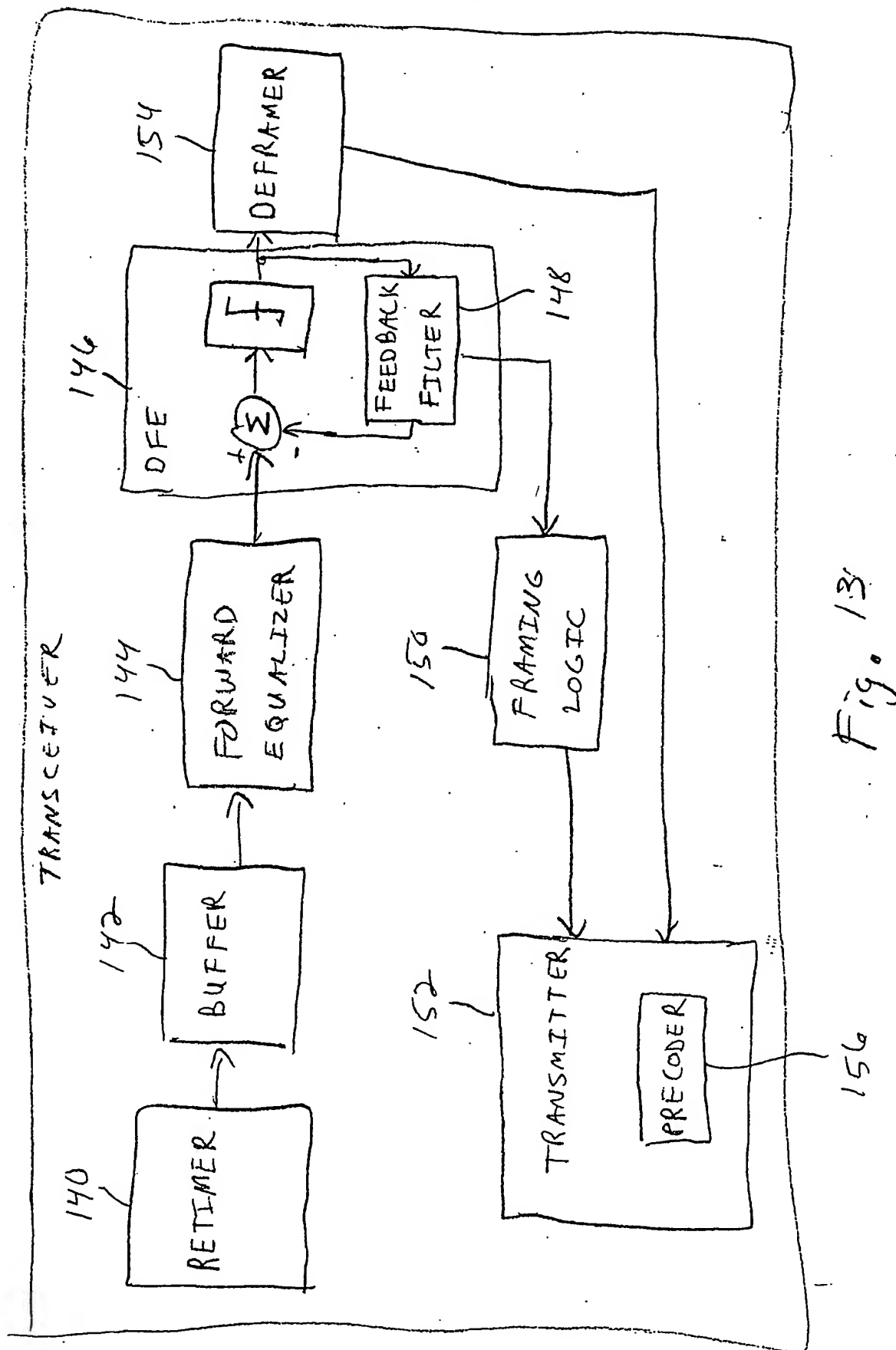


Fig. 13

14/23

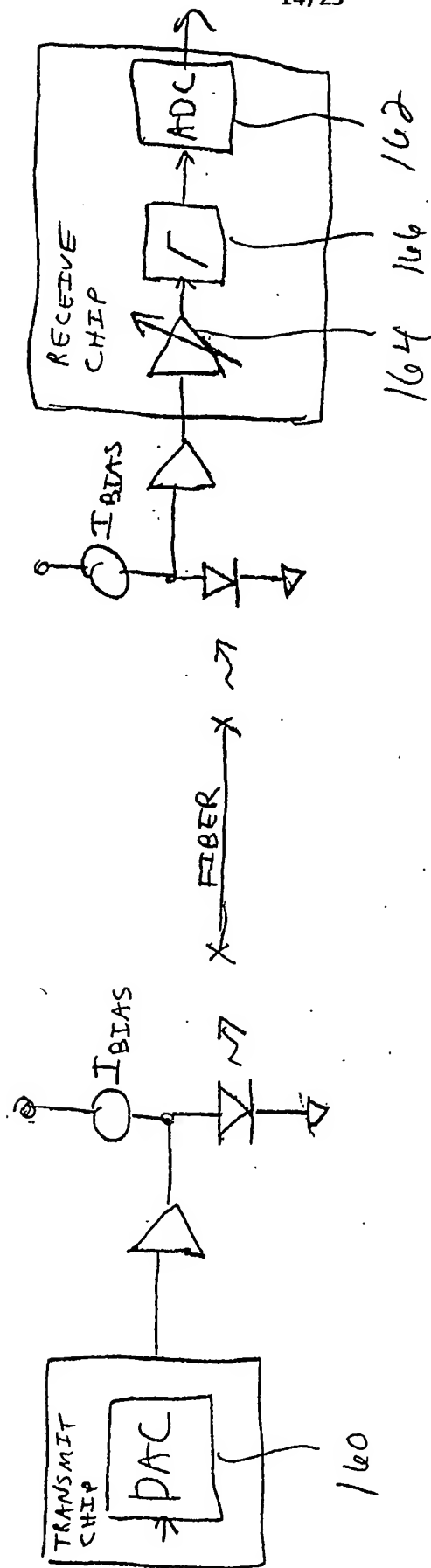


Fig. 14

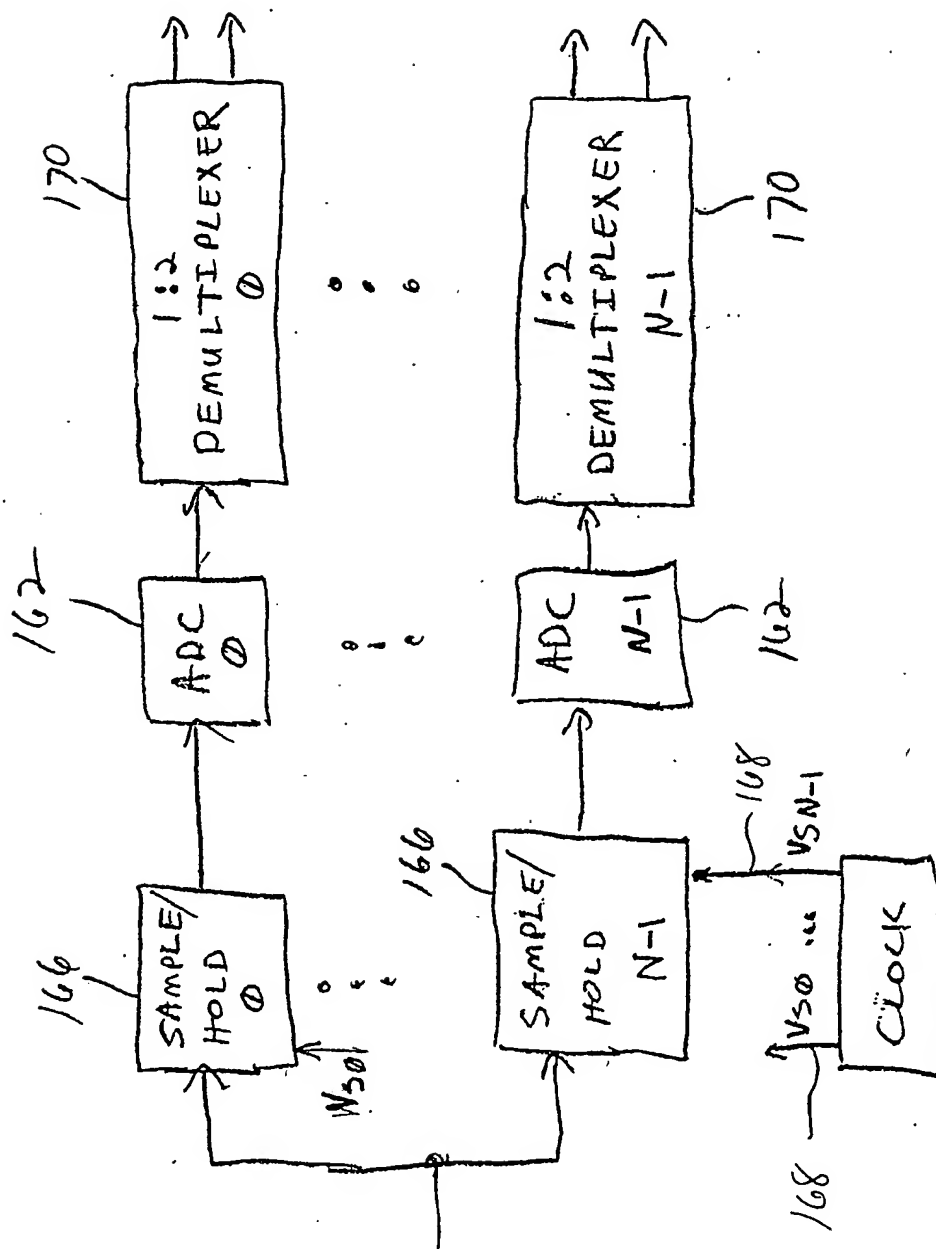


Fig. 15

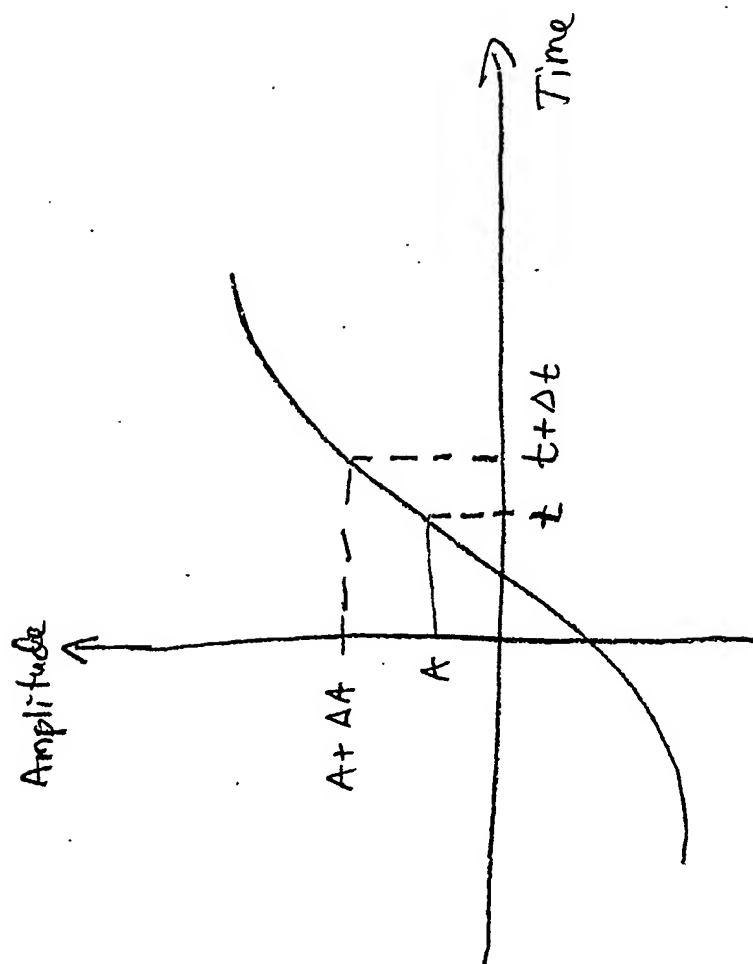


Fig. 16

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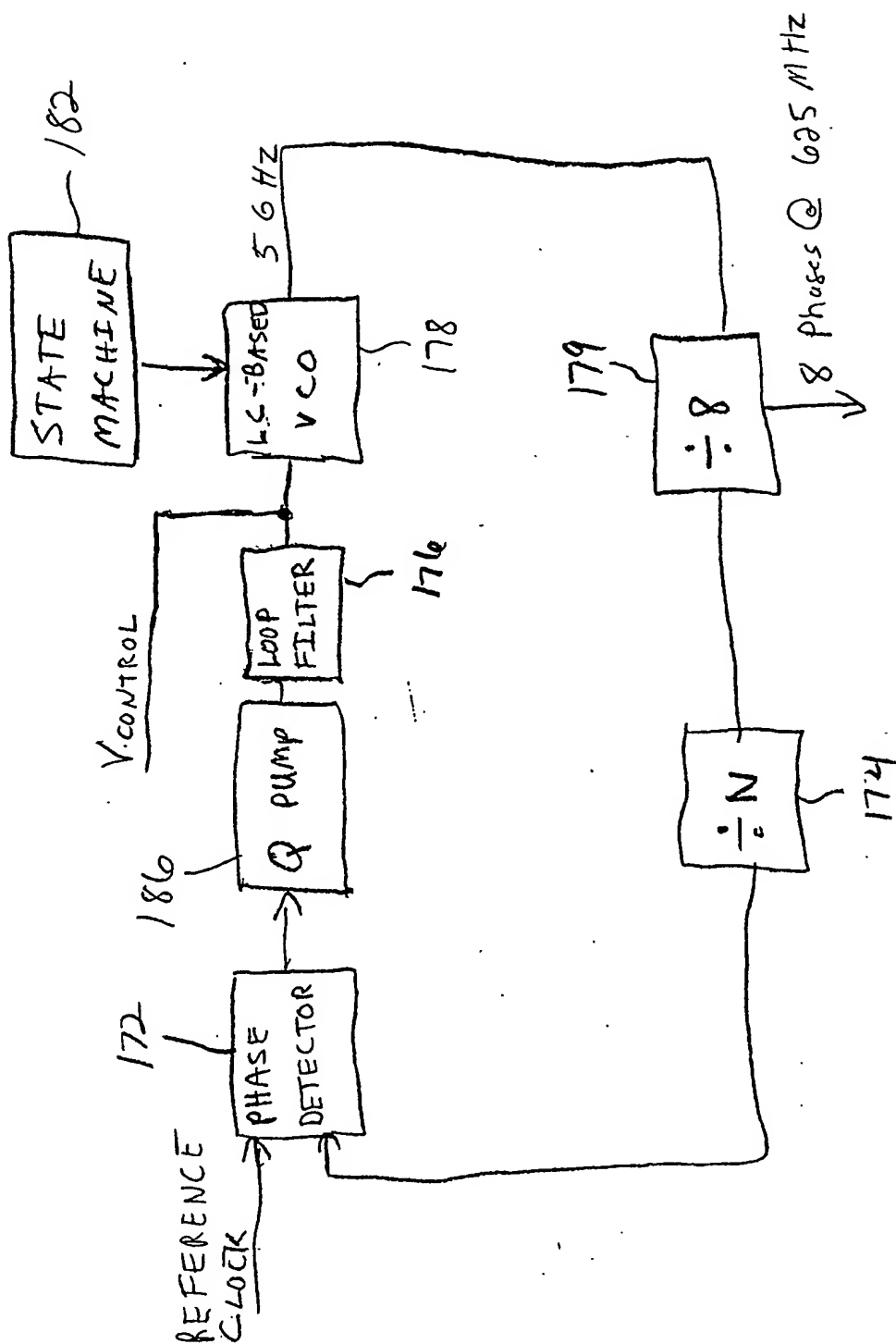


Fig. 17

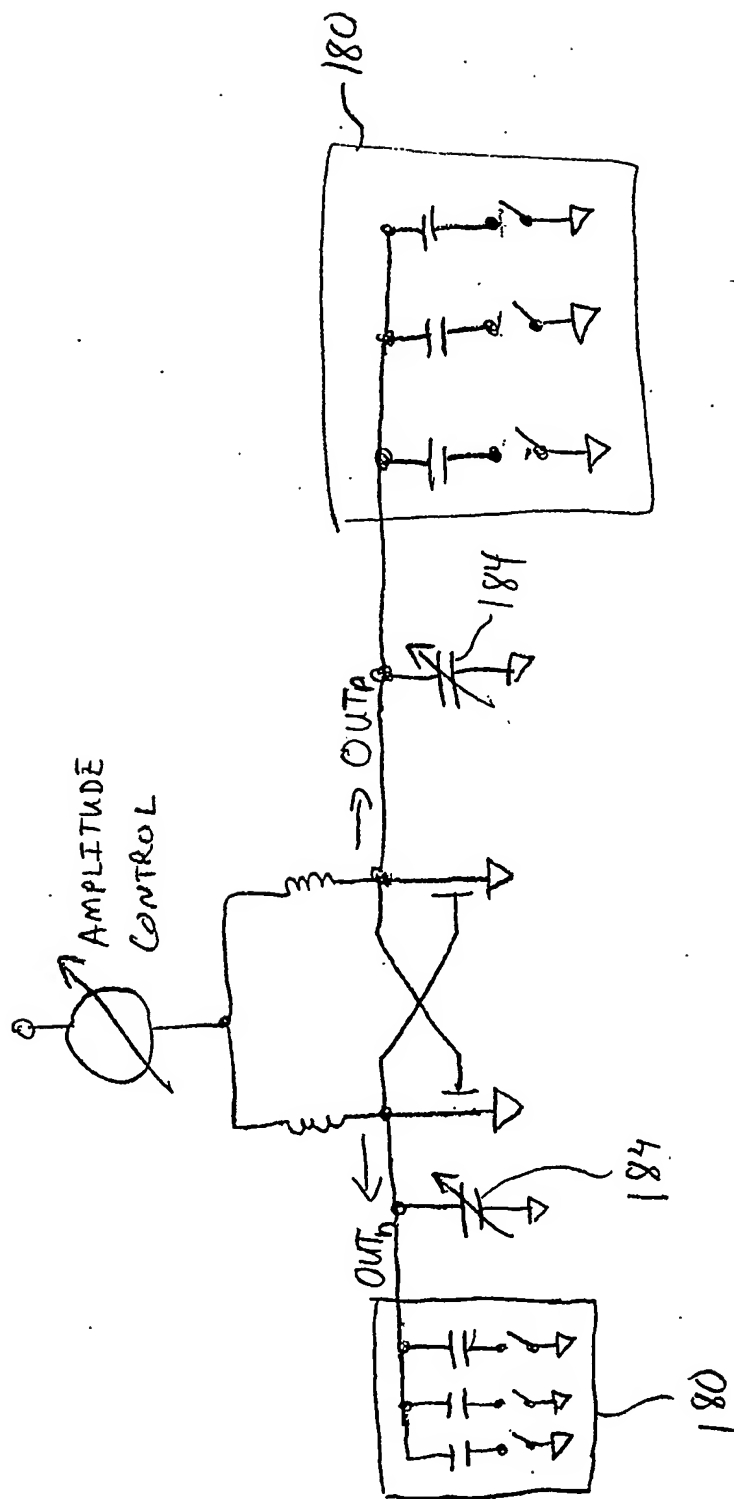


Fig. 18

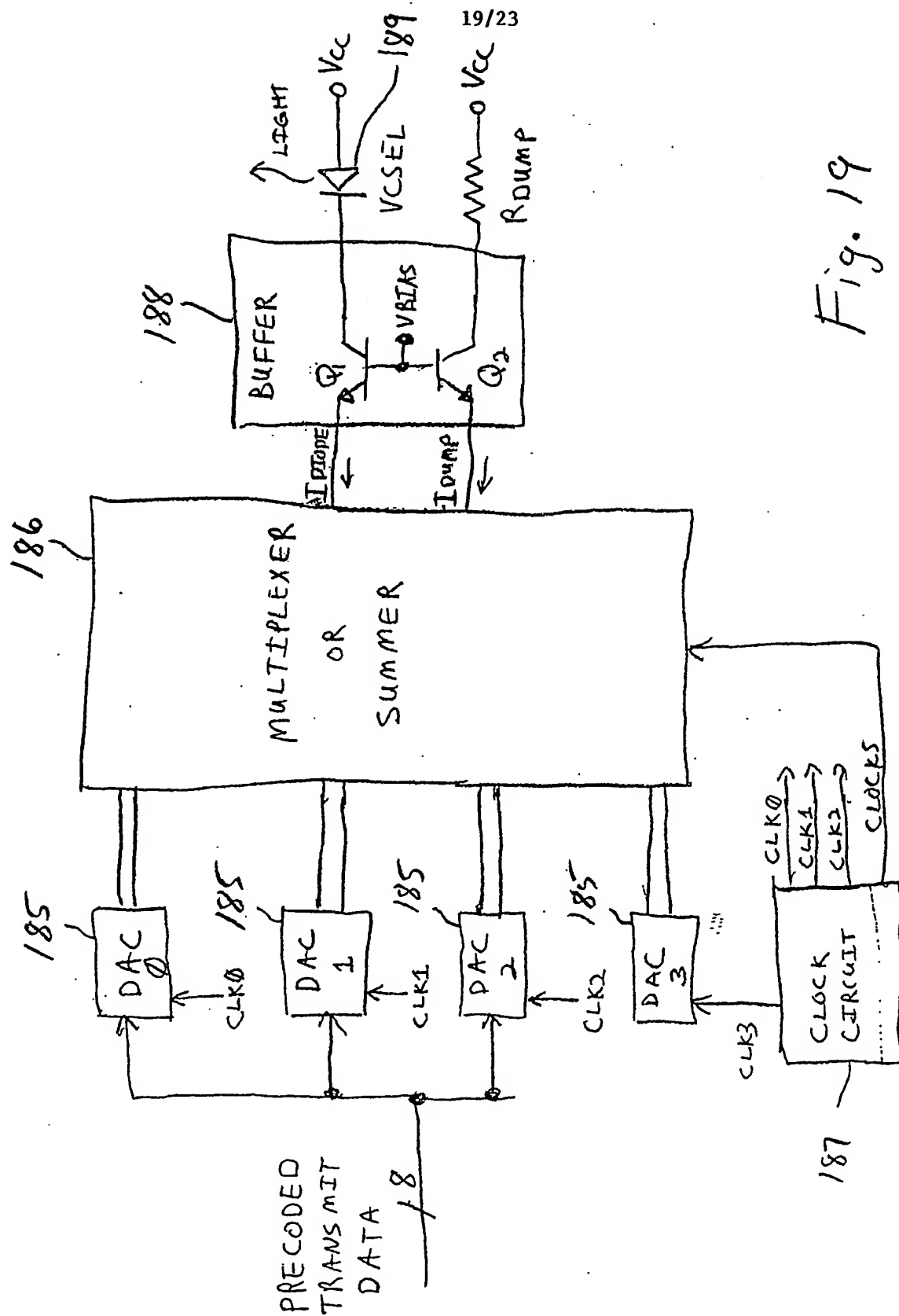


Fig. 19

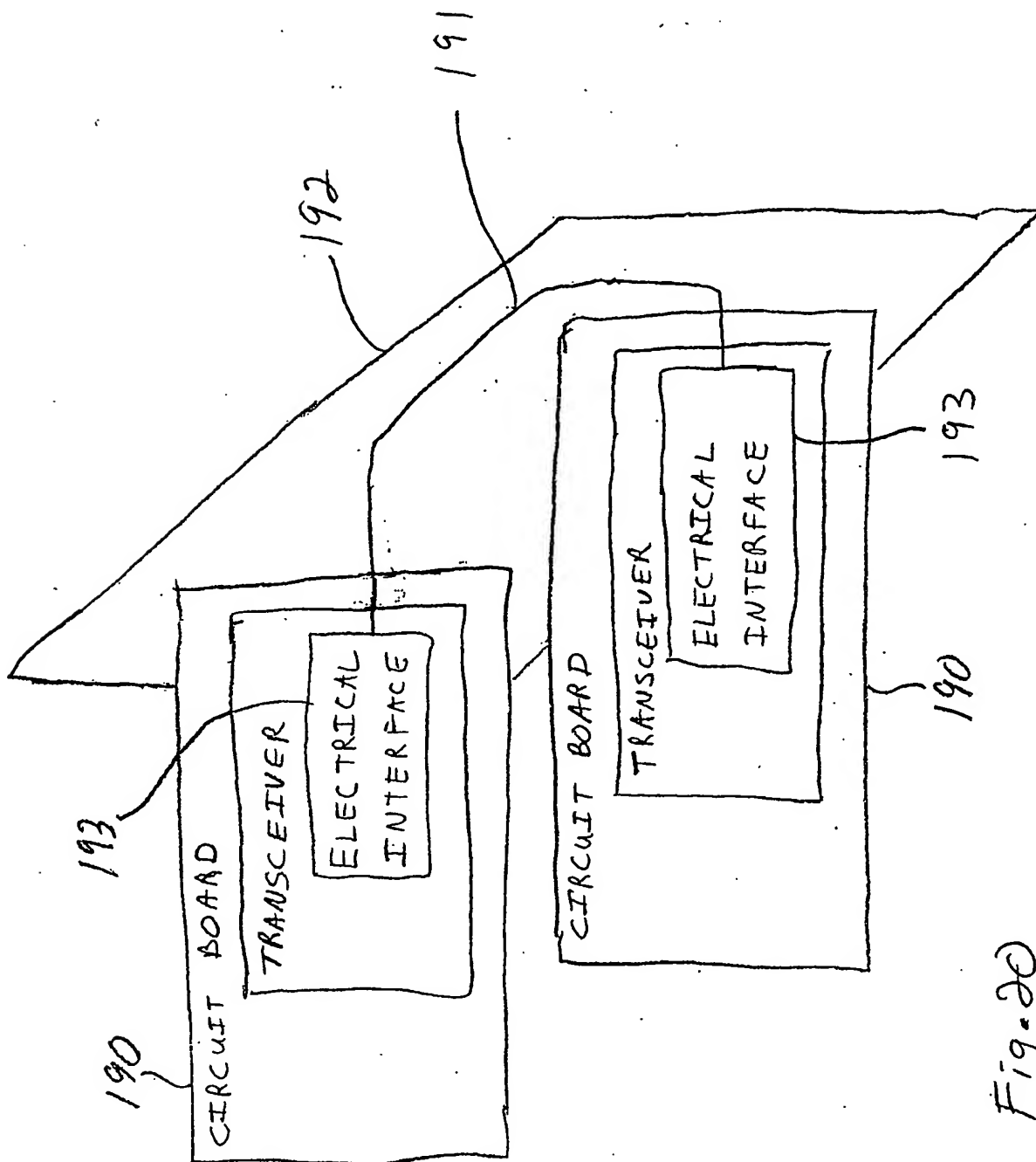


Fig. 20

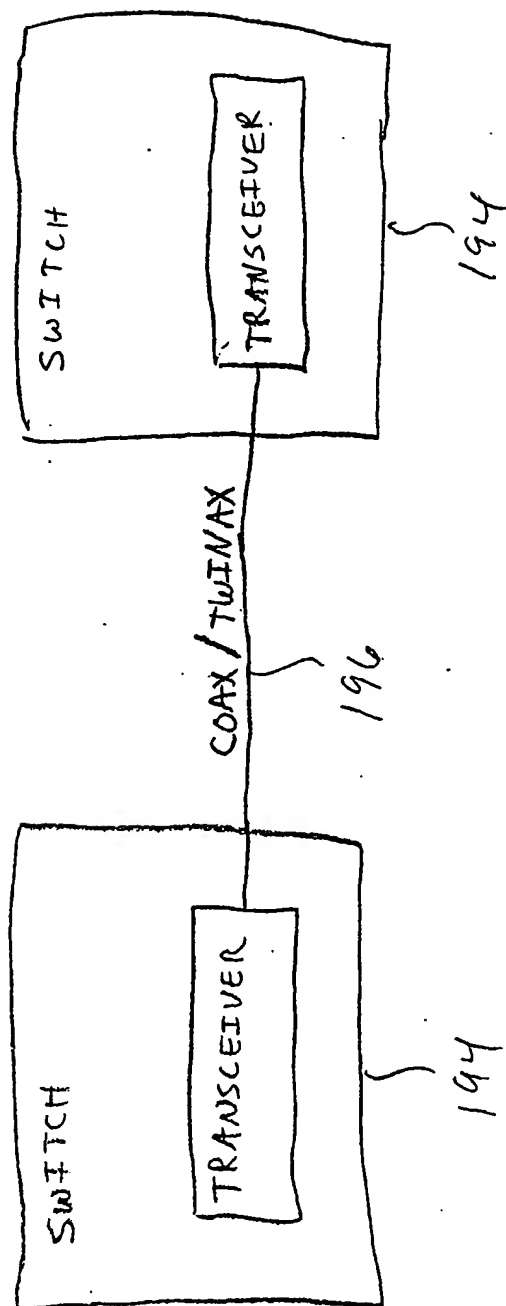


Fig. 21

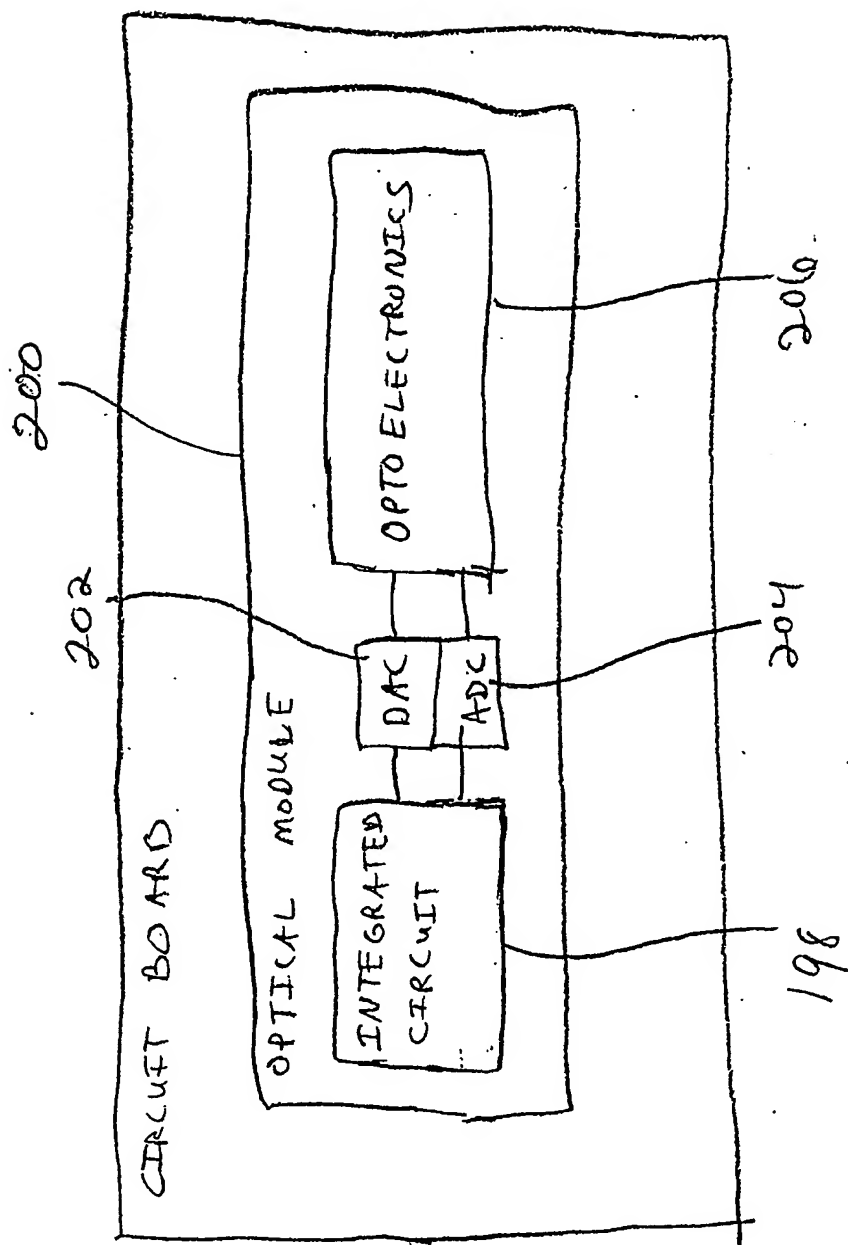


Fig. 22

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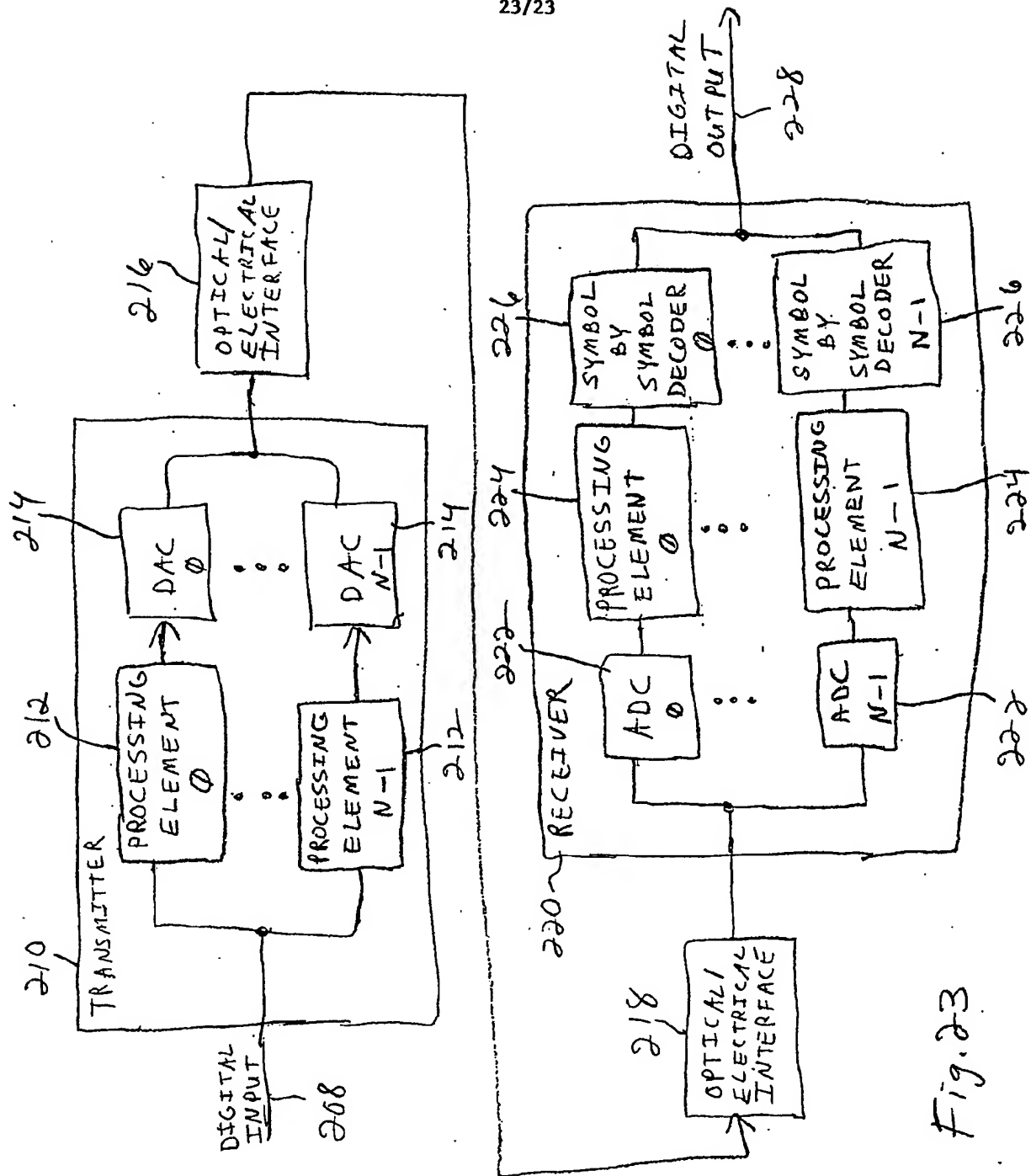


Fig. 23

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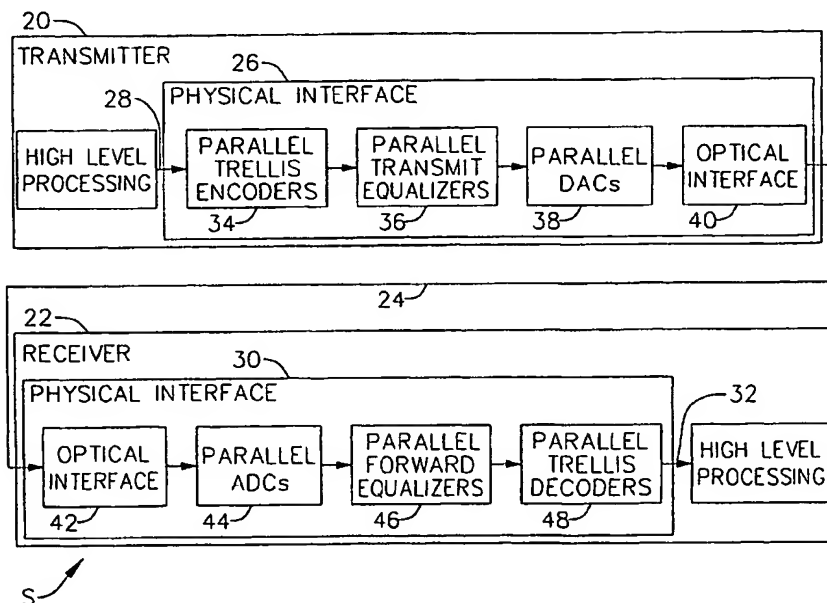
(74) Agent: **BURBACH, Stephen, D.**; Christie, Parker & Hale LLP, P.O. Box 7068, Pasadena, CA 91109-7068 (US).

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[Continued on next page]

(54) Title: SYSTEM AND METHOD FOR HIGH SPEED COMMUNICATIONS USING DIGITAL SIGNAL PROCESSING



(57) Abstract: Various systems and methods related to equalization precoding in a communications channel are disclosed. In one implementation precoding is performed on signals transmitted over an optical channel. In one implementation precoding and decoding operations are performed in parallel to facilitate high speed processing in relatively low cost circuits. Initialization of the precoders may be realized by transmitting information related to the characteristics of the channel between transceiver pairs.

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PCT/US 01/06776

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC, IBM-TDB, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 98 39871 A (LEVEL ONE COMMUNICATIONS INC) 11 September 1998 (1998-09-11) abstract; figure 3 page 1, line 6 - line 8 page 3, line 17 - line 28 ---	1-38
X	EP 0 506 094 A (HITACHI LTD) 30 September 1992 (1992-09-30) page 2, line 9 - line 15 page 3, line 12 - line 18 page 3, line 51 -page 4, column 2 page 6, line 46 -page 7, line 9 page 7, line 29 -page 8, line 3 --- -/--	1-38

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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

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A	<p>KANG J U ET AL: "Highly parallel pulsed optoelectronic analog-digital converter" IEEE PHOTONICS TECHNOLOGY LETTERS, NOV. 1998, IEEE, USA, vol. 10, no. 11, pages 1626-1628, XP002177540 ISSN: 1041-1135 abstract paragraph 'INTRODUCTION!; figure 1 page 1627, column 1, line 6 - line 12</p> <p>-----</p>	14,22,31

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int. :ional Application No

PCT/US 01/06776

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		AU 6685098 A	22-09-1998
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